OIPE IAP93 JUN 29 2001 PATENT & TRADEMARK OFFICE

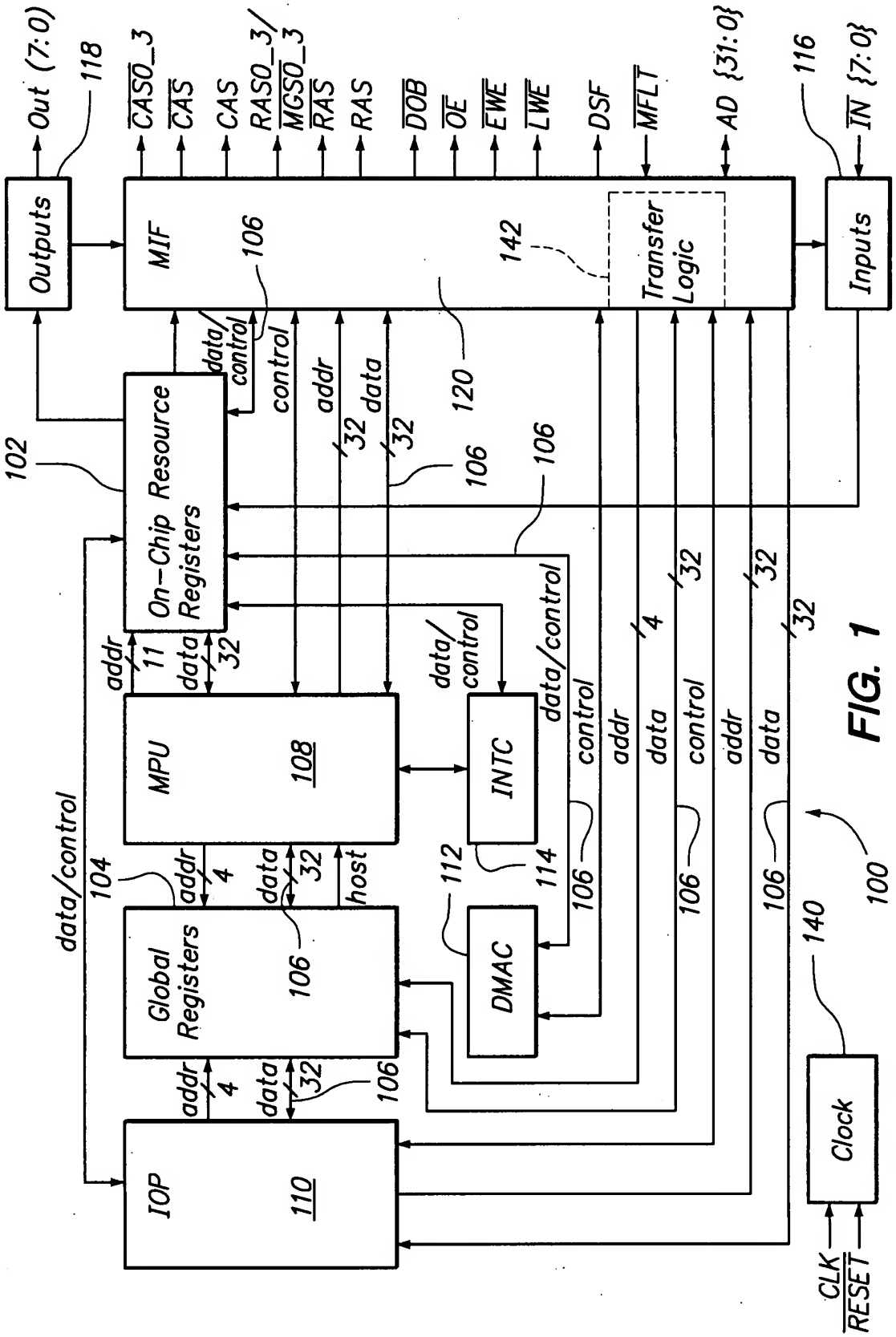


FIG. 1

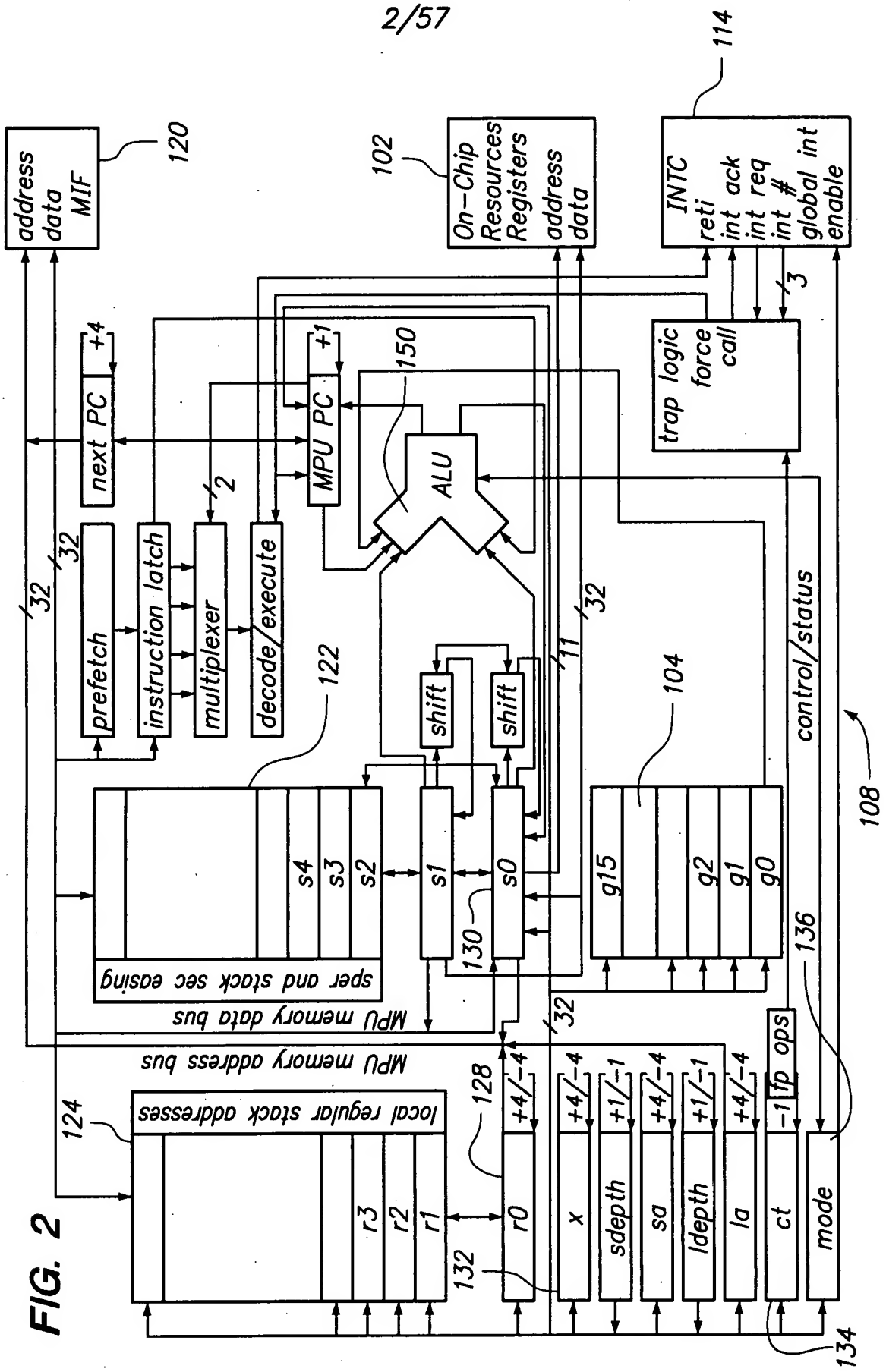

address
data
MIF
120
On-Chip
Resources
Registers
address
data
102
INTC
reti
int ack
int req
int #
global int
enable
114
3
trap logic
force
call
150
next PC
+4
MPU PC
+1
ALU
2
32
prefetch
instruction latch
multiplexer
decode/execute
122
shift
shift
11
32
104
control/status
108
s4
s3
s2
s1
s0
g15
g2
g1
g0
130
136
super and stack sec easing
MPU memory data bus
32
MPU memory address bus
128
+4/-4
+4/-4
+1/-1
+4/-4
+1/-1
+4/-4
-1
fp ops
local regular stack addresses
124
r3
r2
r1
r0
x
sdepth
sa
ldepth
la
ct
mode
132
134

FIG. 2

3/57

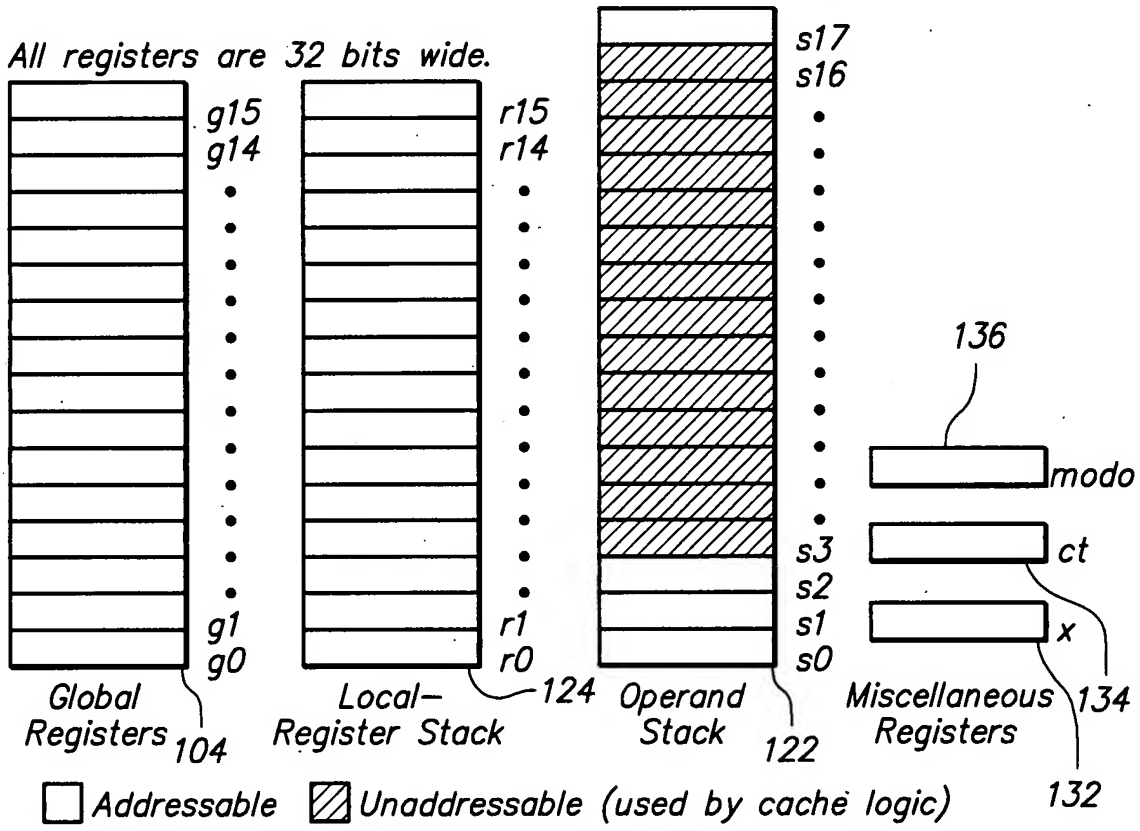


FIG. 3

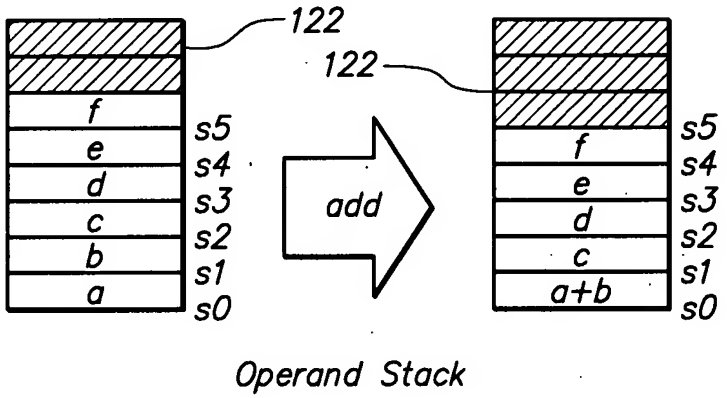


FIG. 3A

4/57

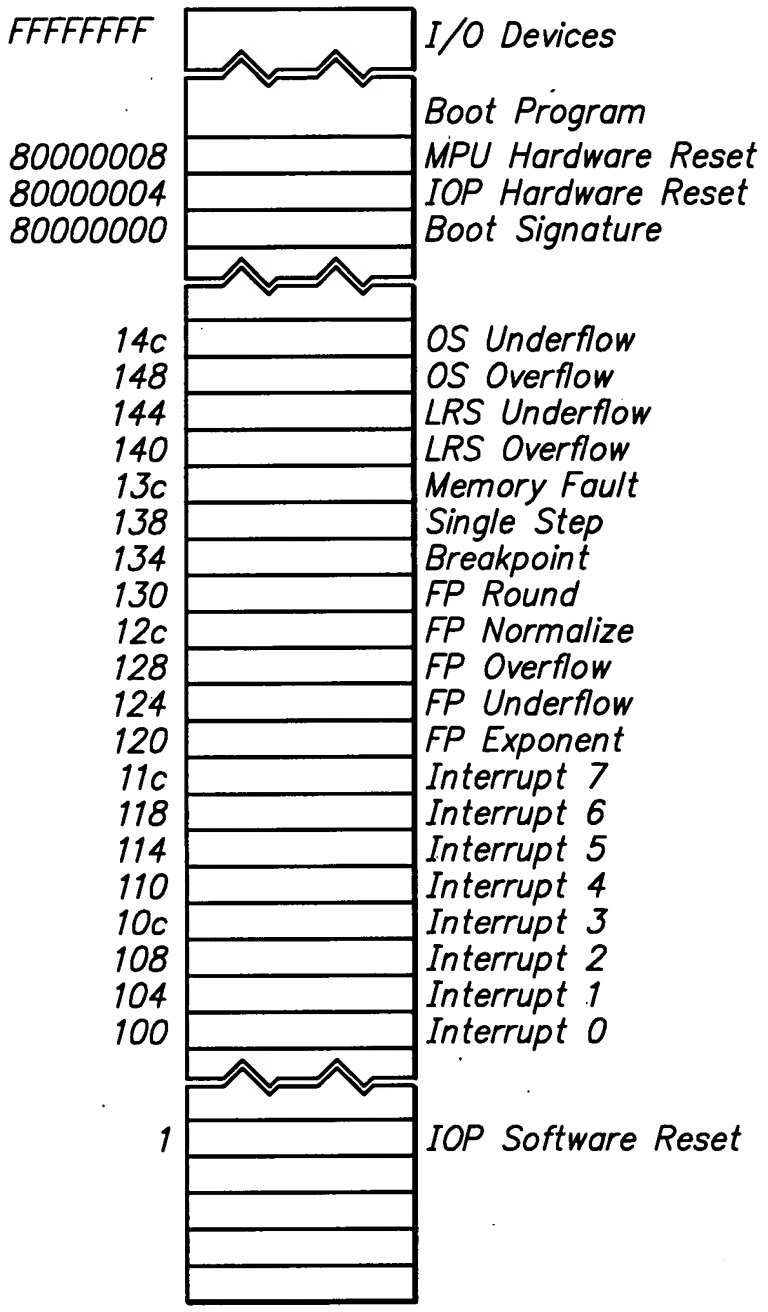

FFFFFFFF
I/O Devices
Boot Program
80000008
MPU Hardware Reset
80000004
IOP Hardware Reset
80000000
Boot Signature
14c
OS Underflow
148
OS Overflow
144
LRS Underflow
140
LRS Overflow
13c
Memory Fault
138
Single Step
134
Breakpoint
130
FP Round
12c
FP Normalize
128
FP Overflow
124
FP Underflow
120
FP Exponent
11c
Interrupt 7
118
Interrupt 6
114
Interrupt 5
110
Interrupt 4
10c
Interrupt 3
108
Interrupt 2
104
Interrupt 1
100
Interrupt 0
1
IOP Software Reset

FIG. 4

5/57

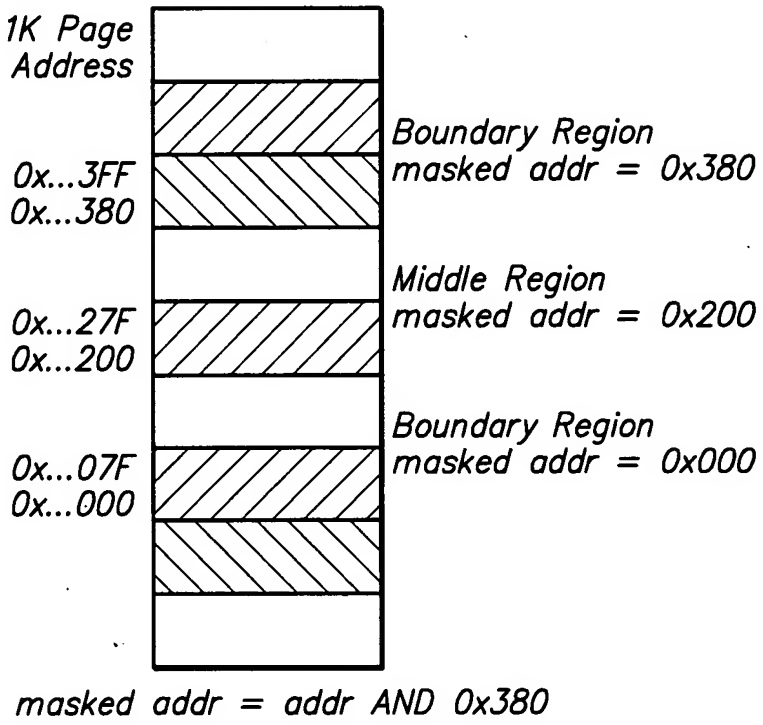


FIG. 5

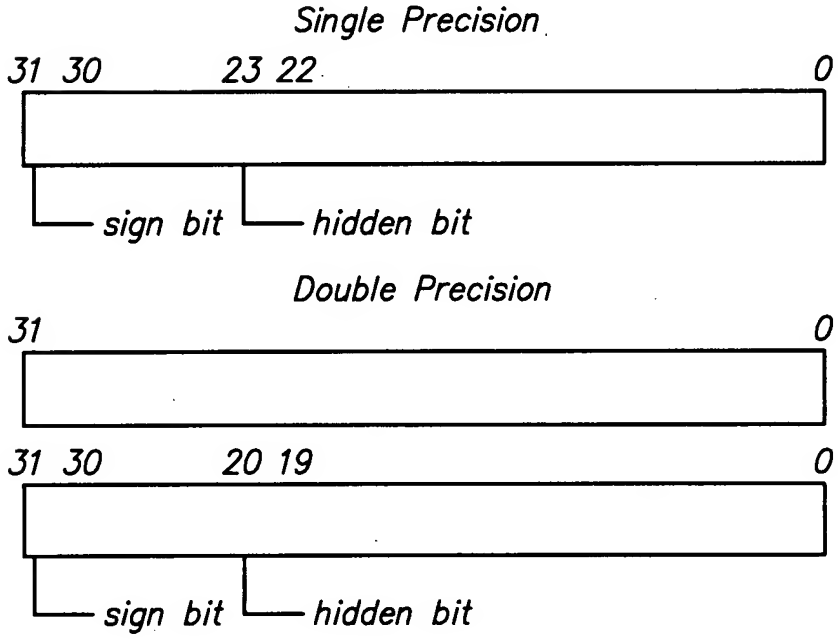


FIG. 6A

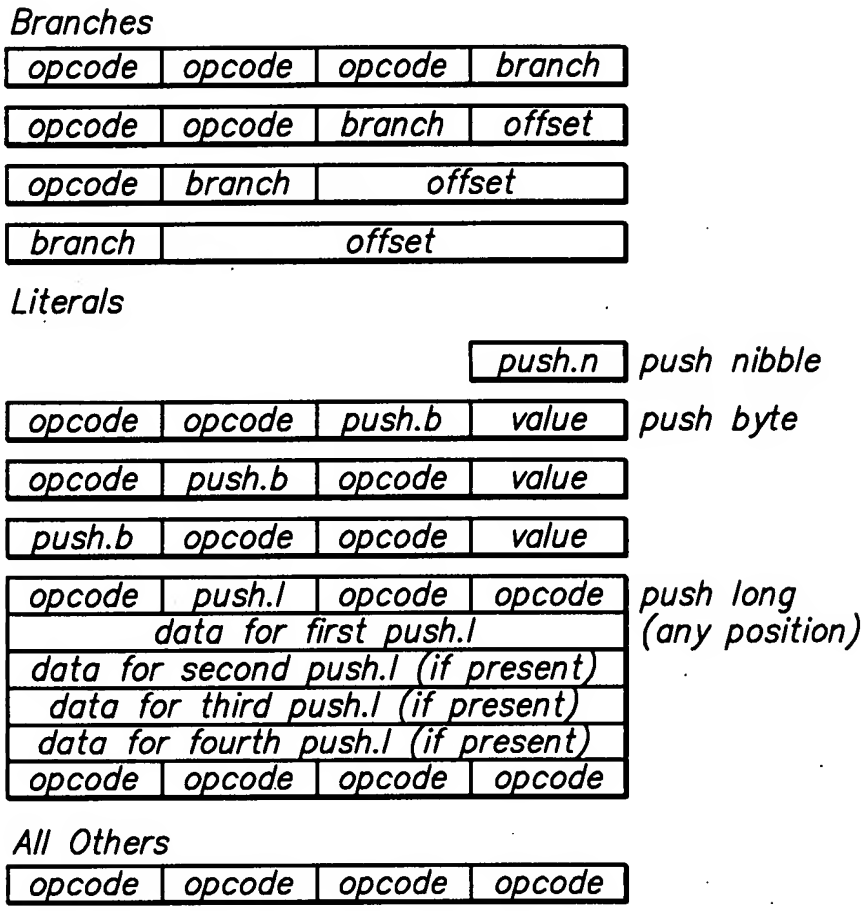
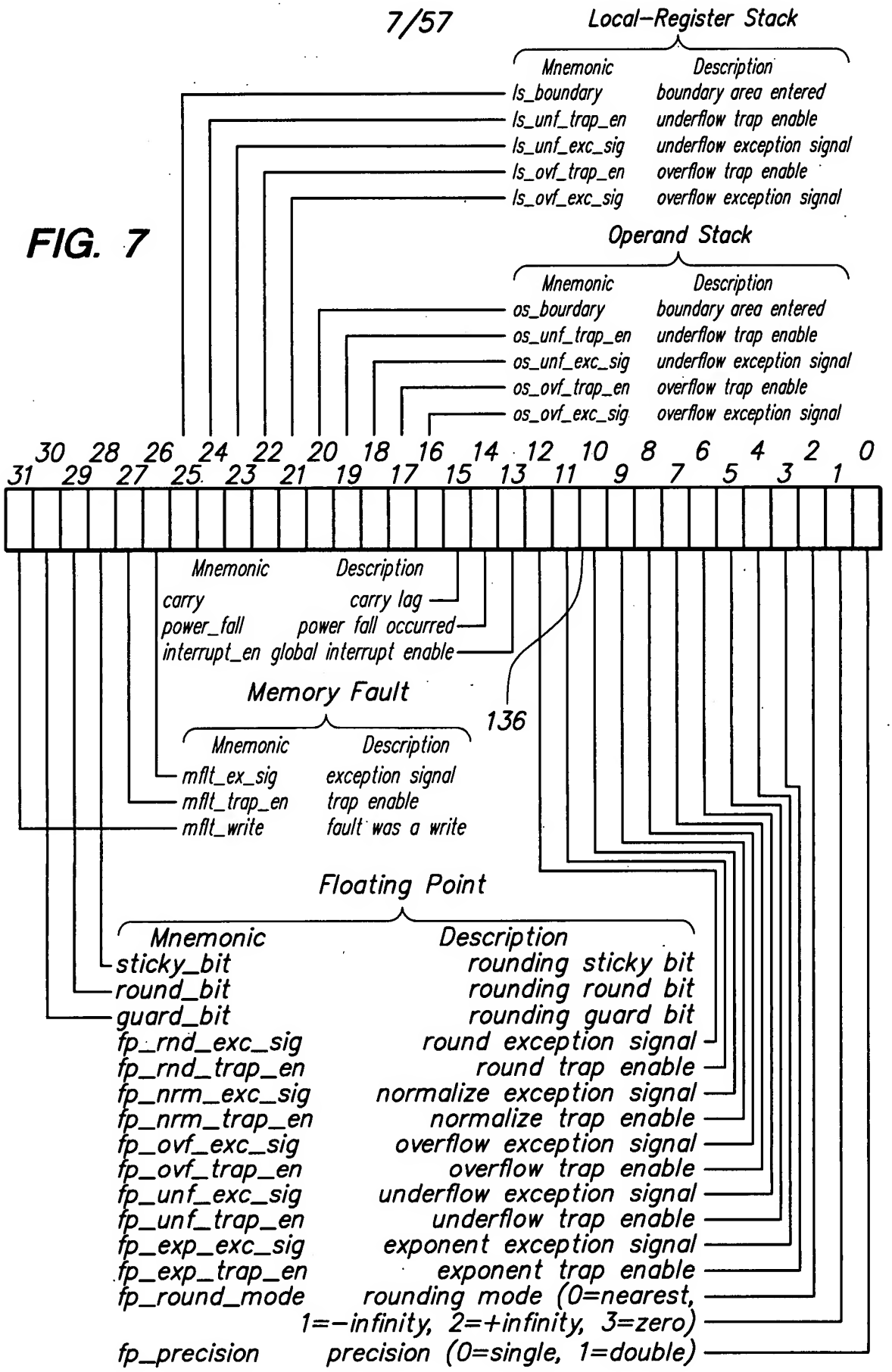

Branches
opcode opcode opcode branch
opcode opcode branch offset
opcode branch offset
branch offset
Literals
push.n
push nibble
opcode opcode push.b value
push byte
opcode push.b opcode value
push.b opcode opcode value
opcode push.l opcode opcode
push long
(any position)
data for first push.l
data for second push.l (if present)
data for third push.l (if present)
data for fourth push.l (if present)
opcode opcode opcode opcode
All Others
opcode opcode opcode opcode

FIG. 6

7/57

FIG. 7


Local–Register Stack
Mnemonic
Description
ls_boundary
boundary area entered
ls_unf_trap_en
underflow trap enable
ls_unf_exc_sig
underflow exception signal
ls_ovf_trap_en
overflow trap enable
ls_ovf_exc_sig
overflow exception signal
Operand Stack
Mnemonic
Description
os_bourdary
boundary area entered
os_unf_trap_en
underflow trap enable
os_unf_exc_sig
underflow exception signal
os_ovf_trap_en
overflow trap enable
os_ovf_exc_sig
overflow exception signal
31 29 27 25 23 21 19 17 15 13 11 9 7 5 3 1
30 28 26 24 22 20 18 16 14 12 10 8 6 4 2 0
Mnemonic
Description
carry
carry lag
power_fall
power fall occurred
interrupt_en
global interrupt enable
Memory Fault
136
Mnemonic
Description
mflt_ex_sig
exception signal
mflt_trap_en
trap enable
mflt_write
fault was a write
Floating Point
Mnemonic
Description
sticky_bit
rounding sticky bit
round_bit
rounding round bit
guard_bit
rounding guard bit
fp_rnd_exc_sig
round exception signal
fp_rnd_trap_en
round trap enable
fp_nrm_exc_sig
normalize exception signal
fp_nrm_trap_en
normalize trap enable
fp_ovf_exc_sig
overflow exception signal
fp_ovf_trap_en
overflow trap enable
fp_unf_exc_sig
underflow exception signal
fp_unf_trap_en
underflow trap enable
fp_exp_exc_sig
exponent exception signal
fp_exp_trap_en
exponent trap enable
fp_round_mode
rounding mode (0=nearest, 1=–infinity, 2=+infinity, 3=zero)
fp_precision
precision (0=single, 1=double)

8/57

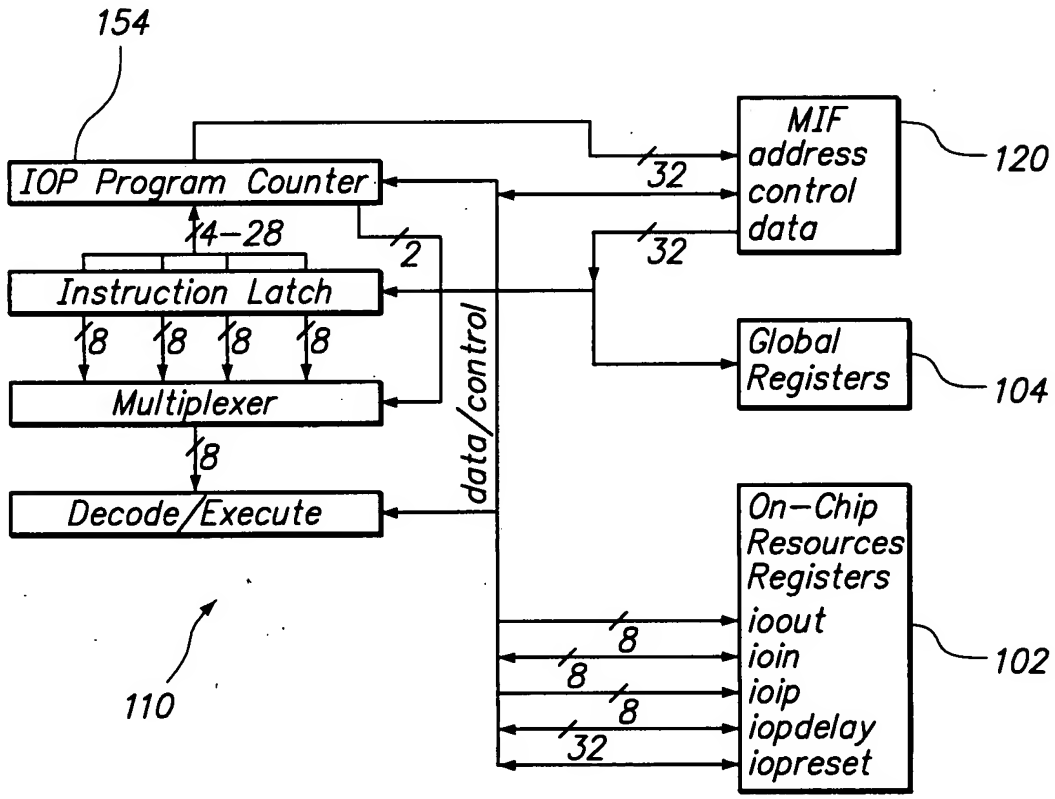


FIG. 8

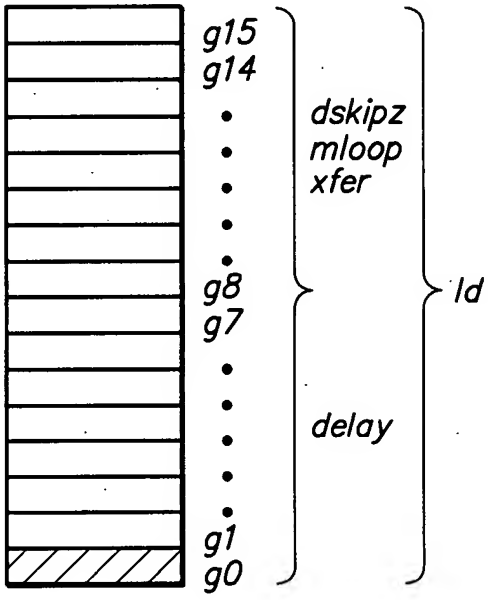


FIG. 9

9/57

Branches

opcode	opcode	opcode	branch
opcode	opcode	branch	offset
opcode	branch	offset	
branch	offset		

Literals

opcode	Id #,gn	opcode	opcode	load register (any position)
data for first Id #,gn				
data for second Id #,gn (if present)				
data for third Id #,gn (if present)				
data for fourth Id #,gn (if present)				
opcode	opcode	opcode	opcode	

All Others

opcode	opcode	opcode	opcode

FIG. 10

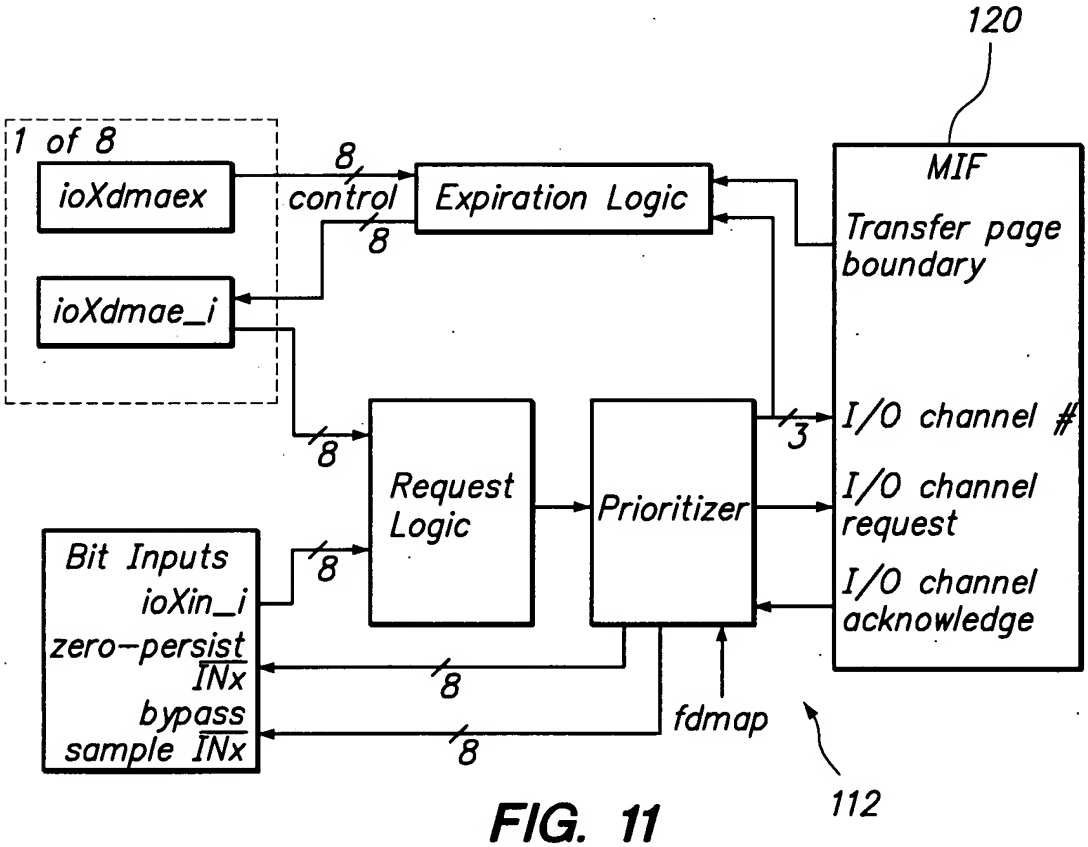


FIG. 11

10/57

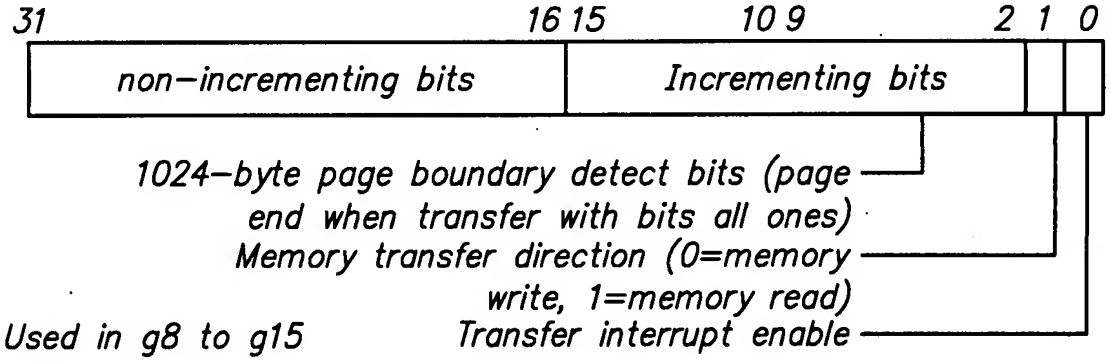


FIG. 12

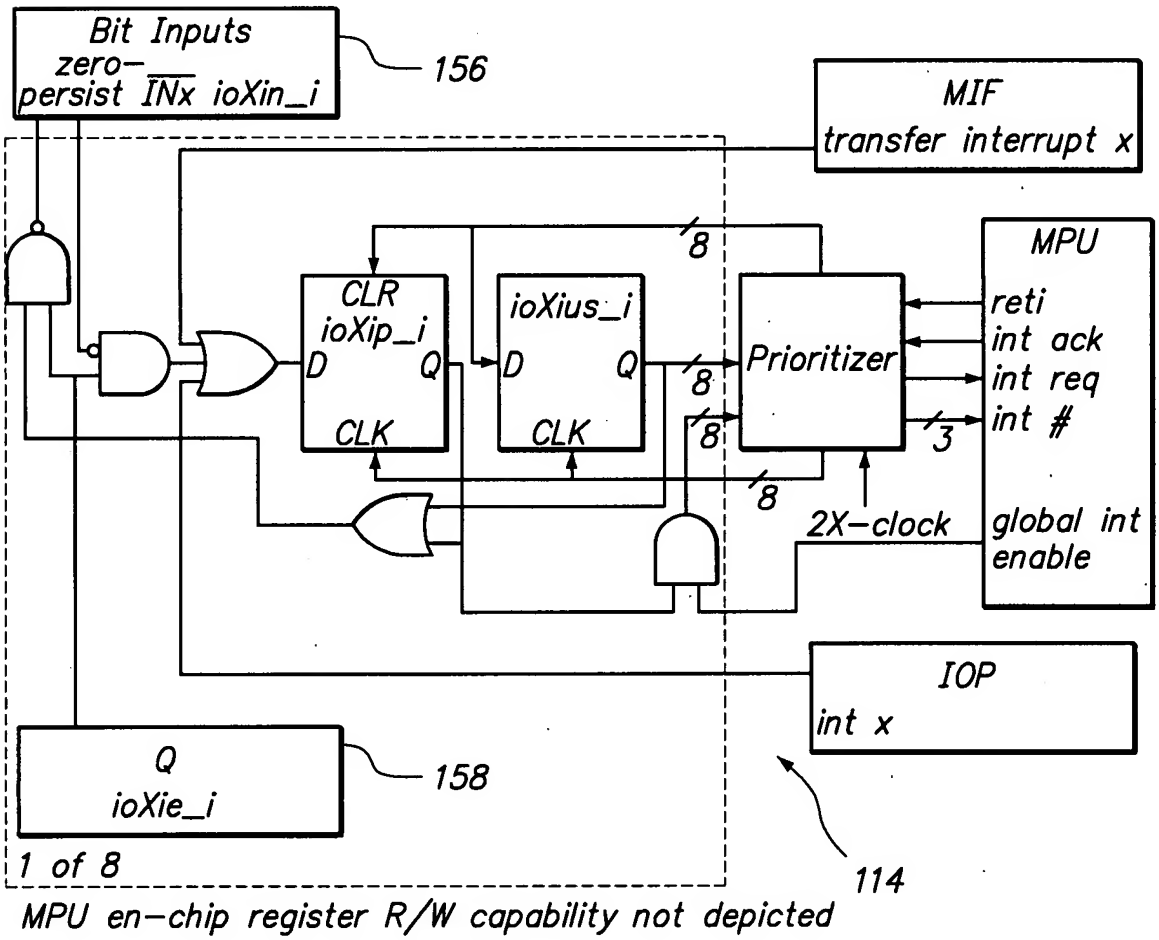


FIG. 13

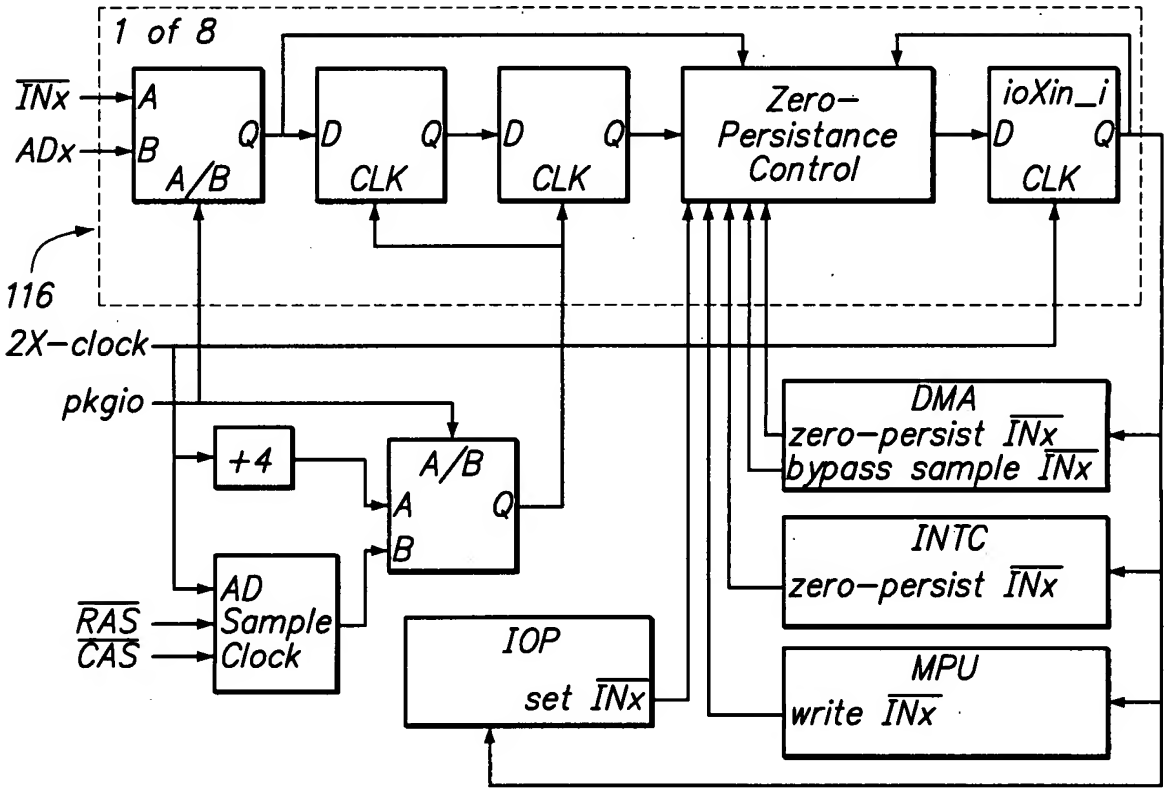

1 of 8
INx
ADx
A
B
A/B
Q
D
CLK
Zero-
Persistance
Control
ioXin_i
116
2X-clock
pkgio
+4
AD
Sample
Clock
RAS
CAS
DMA
zero-persist INx
bypass sample INx
INTC
zero-persist INx
IOP
set INx
MPU
write INx

FIG. 14

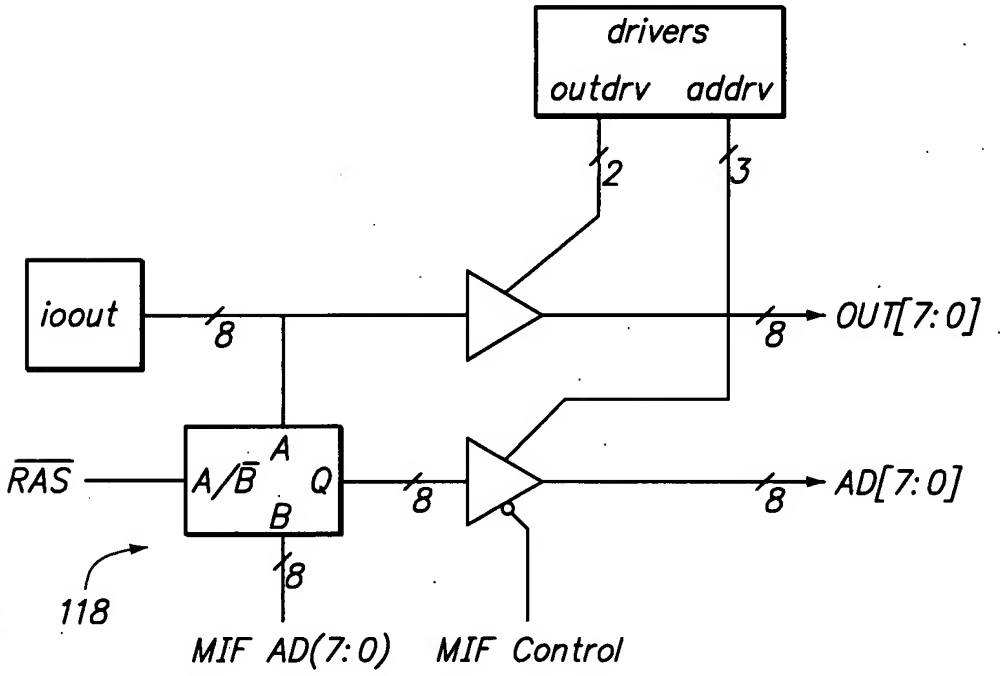
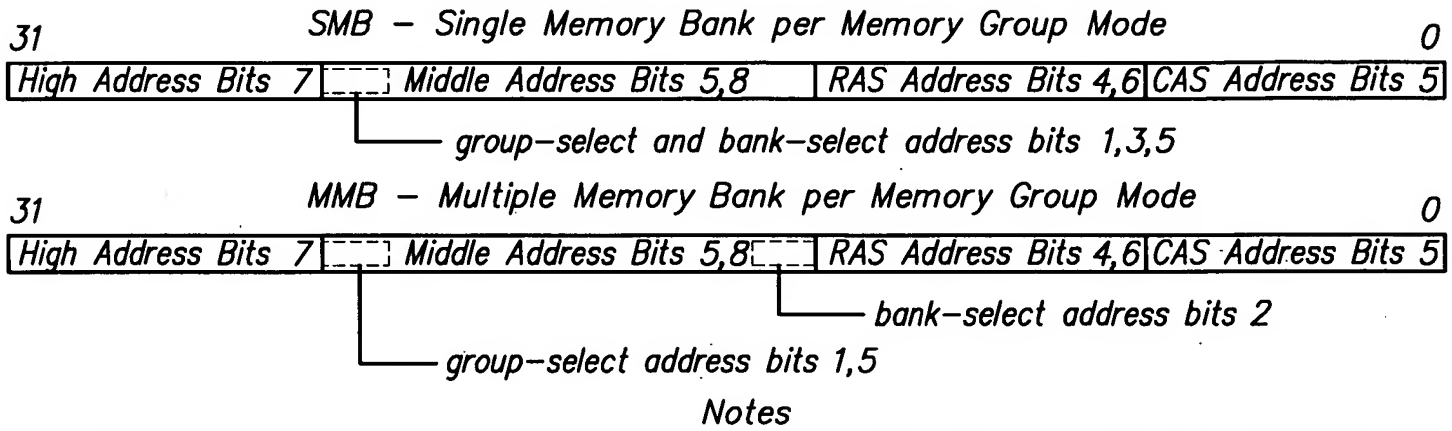

drivers
outdrv
addrv
2
3
ioout
8
OUT[7:0]
RAS
A/B
A
B
Q
AD[7:0]
118
MIF AD(7:0)
MIF Control

FIG. 15



Notes

1. Located by bits in msgsm.
2. DRAM–2 bits immediately above the RAS address bits. SRAM–2 bits located by mssbs in miscc.
3. SRAM and DRAM.
4. DRAM only, field is zero length in SRAM.
5. Excluded from RAS–cycle determination, except for A31 (see note 7).
6. Included in RAS–cycle determination.
7. Optionally included in RAS–cycle determination.
8. If msgsm is zero, see text.

FIG. 16

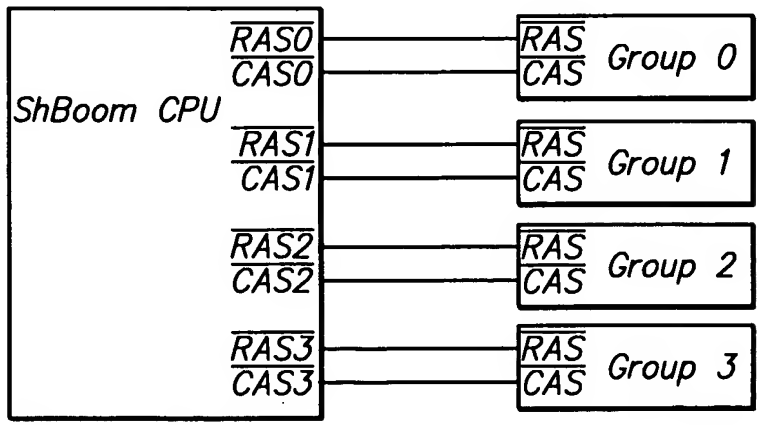


FIG. 17

13/57

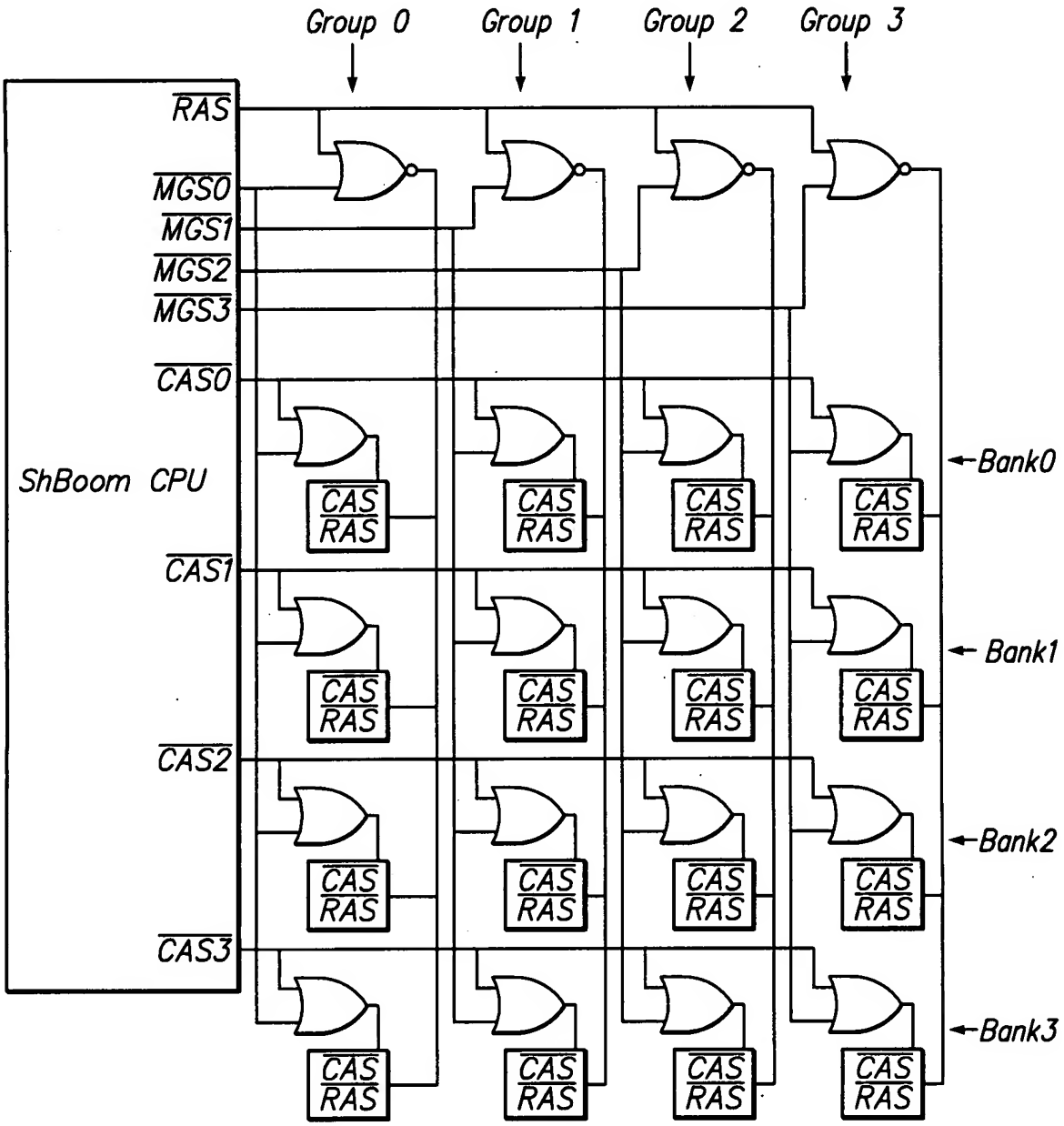

Group 0
Group 1
Group 2
Group 3
RAS
MGS0
MGS1
MGS2
MGS3
CAS0
CAS1
CAS2
CAS3
ShBoom CPU
CAS RAS
Bank0
Bank1
Bank2
Bank3

FIG. 18

14/57

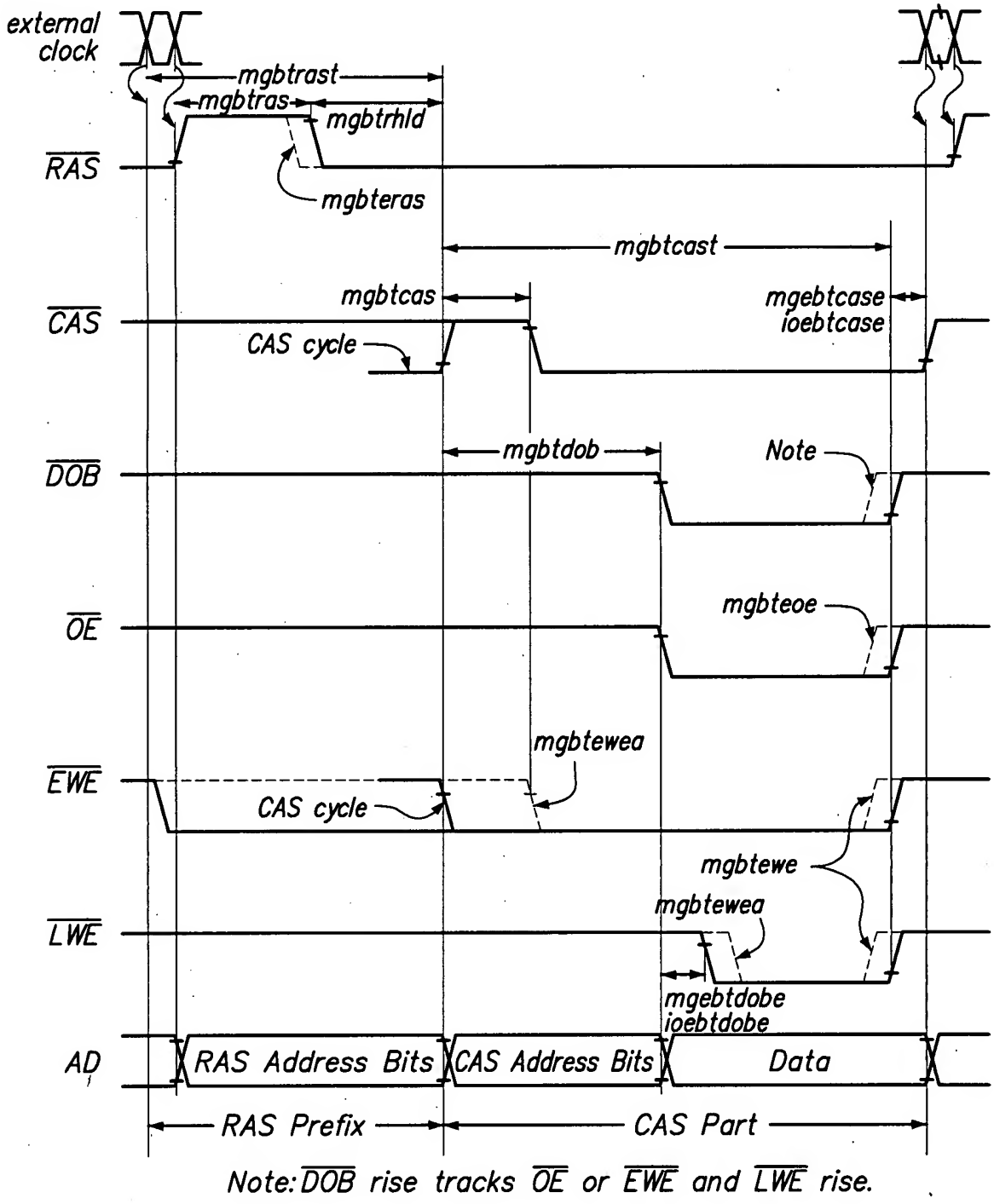
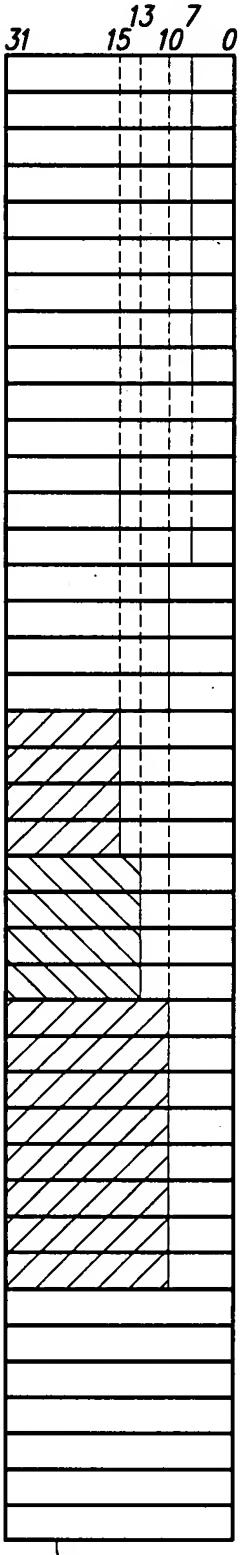

external clock
mgbtrast
mgbtras
mgbtrhld
RAS
mgbteras
mgbtcast
mgbtcas
mgebtcase
ioebtcase
CAS
CAS cycle
mgbtdob
Note
DOB
mgbteoe
OE
mgbtewea
EWE
CAS cycle
mgbtewe
mgbtewea
LWE
mgebtdobe
ioebtdobe
AD
RAS Address Bits
CAS Address Bits
Data
RAS Prefix
CAS Part
Note: DOB rise tracks OE or EWE and LWE rise.

FIG. 19

15/57



Register Size	Addr	Mnemonic	Description
	000	ioin	Bit Input Register
	020	ioip	Interrupt Pending Register
	040	ioius	Interrupt Under Service Register
	060	ioout	Bit Output Register
	080	ioie	Interrupt Enable Register
	0a0	iodmae	DMA Enable Register
	0c0	vram	VRAM Control Bit Register
	0e0	misca	Miscellaneous A Register
	100	miscb	Miscellaneous B Register
	120	mfltaddr	Memory Fault Address Register
	140	mfltdata	Memory Fault Data Register
	160	msgsm	Memory System Group Select Mask Register
	180	mgds	Memory Group Device Size Register
	1a0	miscc	Miscellaneous C Register
	1c0	mg0ebt	Memory Group 0 Extended Bus Timing Register
	1e0	mg1ebt	Memory Group 1 Extended Bus Timing Register
	200	mg2ebt	Memory Group 2 Extended Bus Timing Register
	220	mg3ebt	Memory Group 3 Extended Bus Timing Register
	240	mg0casbt	Memory Group 0 CAS Bus Timing Register
	260	mg1casbt	Memory Group 1 CAS Bus Timing Register
	280	mg2casbt	Memory Group 2 CAS Bus Timing Register
	2a0	mg3casbt	Memory Group 3 CAS Bus Timing Register
	2c0	mg0rasbt	Memory Group 0 RAS Bus Timing Register
	2e0	mg1rasbt	Memory Group 1 RAS Bus Timing Register
	300	mg2rasbt	Memory Group 2 RAS Bus Timing Register
	320	mg3rasbt	Memory Group 3 RAS Bus Timing Register
	340	io0ebt	I/O Channel 0 Extended Bus Timing Register
	360	io1ebt	I/O Channel 1 Extended Bus Timing Register
	380	io2ebt	I/O Channel 2 Extended Bus Timing Register
	3a0	io3ebt	I/O Channel 3 Extended Bus Timing Register
	3c0	io4ebt	I/O Channel 4 Extended Bus Timing Register
	3e0	io5ebt	I/O Channel 5 Extended Bus Timing Register
	400	io6ebt	I/O Channel 6 Extended Bus Timing Register
	420	io7ebt	I/O Channel 7 Extended Bus Timing Register
	440	msra	Memory System Refresh Address Register(WO)
	440	iopdelay	IOP Delay Register(RO)
	460	iodta	I/O Device Transfer Types A Register
	480	iodtb	I/O Device Transfer Types B Register
	7a0	iodmaex	I/O DMA Enable Expiration Register
	7c0	drvera	Driver Current Register
	7e0	iopreset	IOP Reset Register

102

FIG. 20

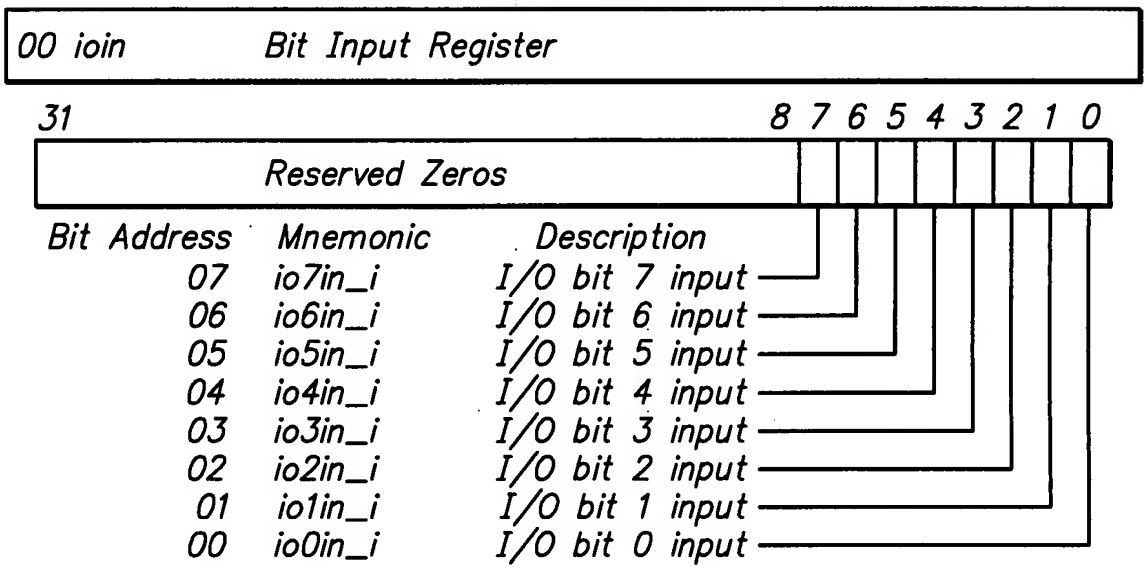

00 ioin
Bit Input Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Bit Address
Mnemonic
Description
07 io7in_i I/O bit 7 input
06 io6in_i I/O bit 6 input
05 io5in_i I/O bit 5 input
04 io4in_i I/O bit 4 input
03 io3in_i I/O bit 3 input
02 io2in_i I/O bit 2 input
01 io1in_i I/O bit 1 input
00 io0in_i I/O bit 0 input

FIG. 21

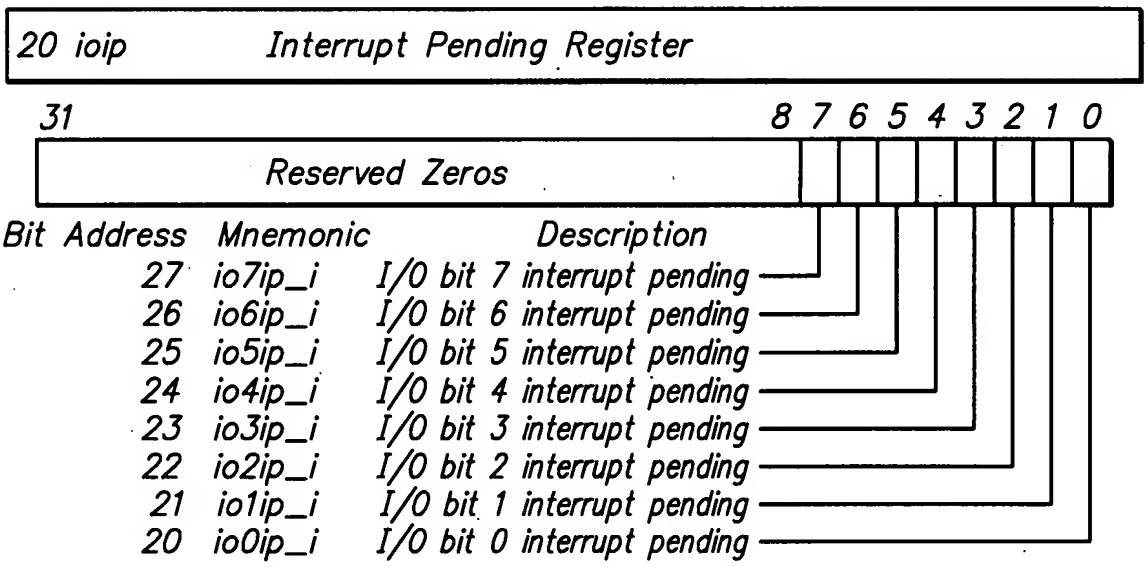

20 ioip
Interrupt Pending Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Bit Address
Mnemonic
Description
27 io7ip_i I/O bit 7 interrupt pending
26 io6ip_i I/O bit 6 interrupt pending
25 io5ip_i I/O bit 5 interrupt pending
24 io4ip_i I/O bit 4 interrupt pending
23 io3ip_i I/O bit 3 interrupt pending
22 io2ip_i I/O bit 2 interrupt pending
21 io1ip_i I/O bit 1 interrupt pending
20 io0ip_i I/O bit 0 interrupt pending

FIG. 22

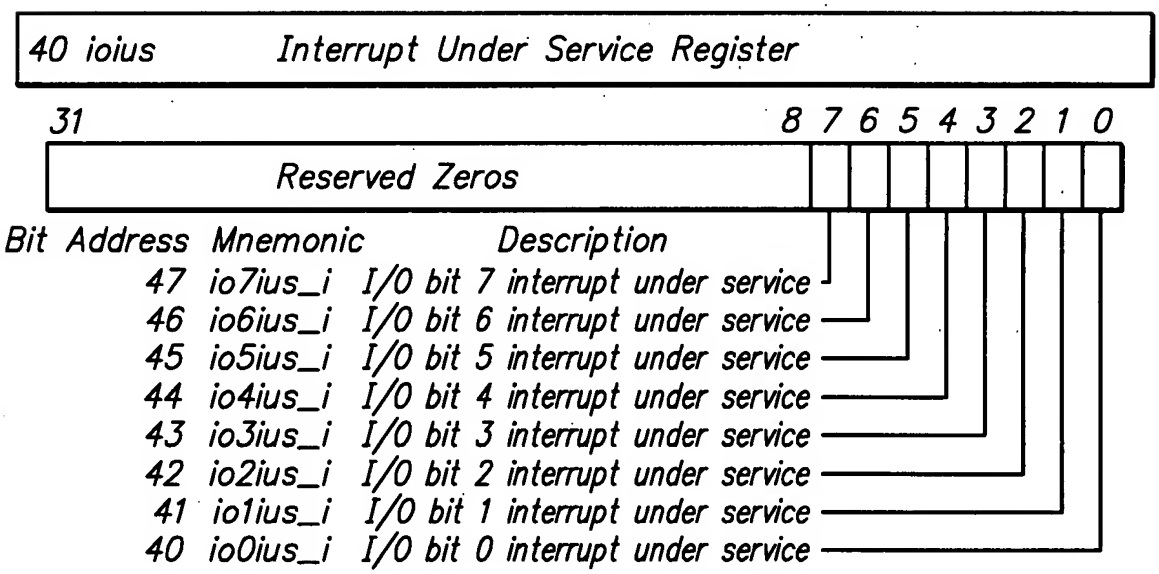

40 ioius Interrupt Under Service Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Bit Address Mnemonic Description
47 io7ius_i I/O bit 7 interrupt under service
46 io6ius_i I/O bit 6 interrupt under service
45 io5ius_i I/O bit 5 interrupt under service
44 io4ius_i I/O bit 4 interrupt under service
43 io3ius_i I/O bit 3 interrupt under service
42 io2ius_i I/O bit 2 interrupt under service
41 io1ius_i I/O bit 1 interrupt under service
40 io0ius_i I/O bit 0 interrupt under service

FIG. 23

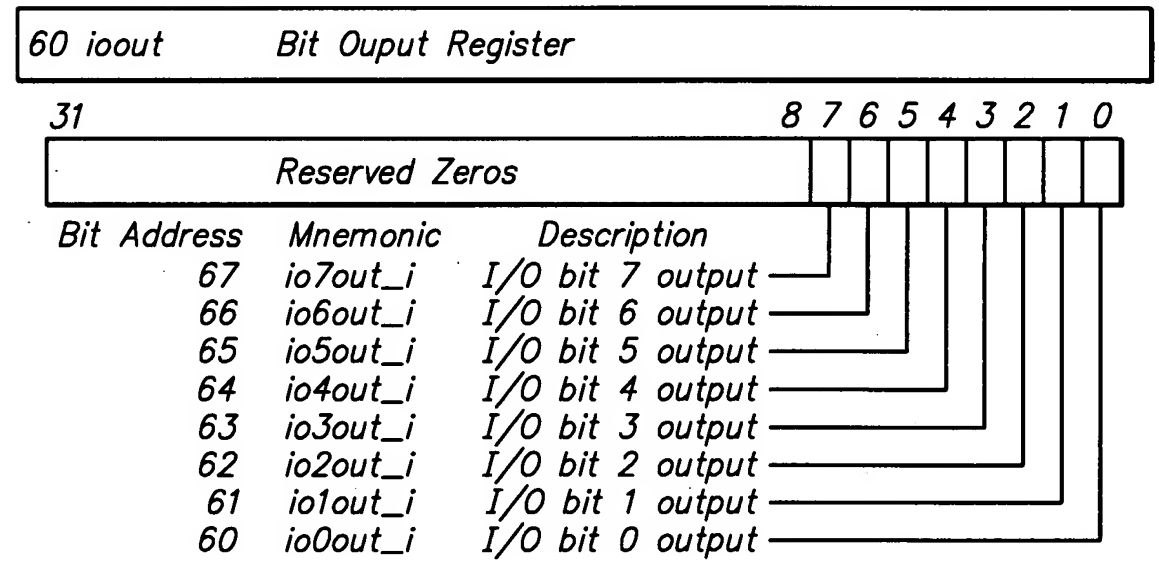

60 ioout Bit Ouput Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Bit Address Mnemonic Description
67 io7out_i I/O bit 7 output
66 io6out_i I/O bit 6 output
65 io5out_i I/O bit 5 output
64 io4out_i I/O bit 4 output
63 io3out_i I/O bit 3 output
62 io2out_i I/O bit 2 output
61 io1out_i I/O bit 1 output
60 io0out_i I/O bit 0 output

FIG. 24

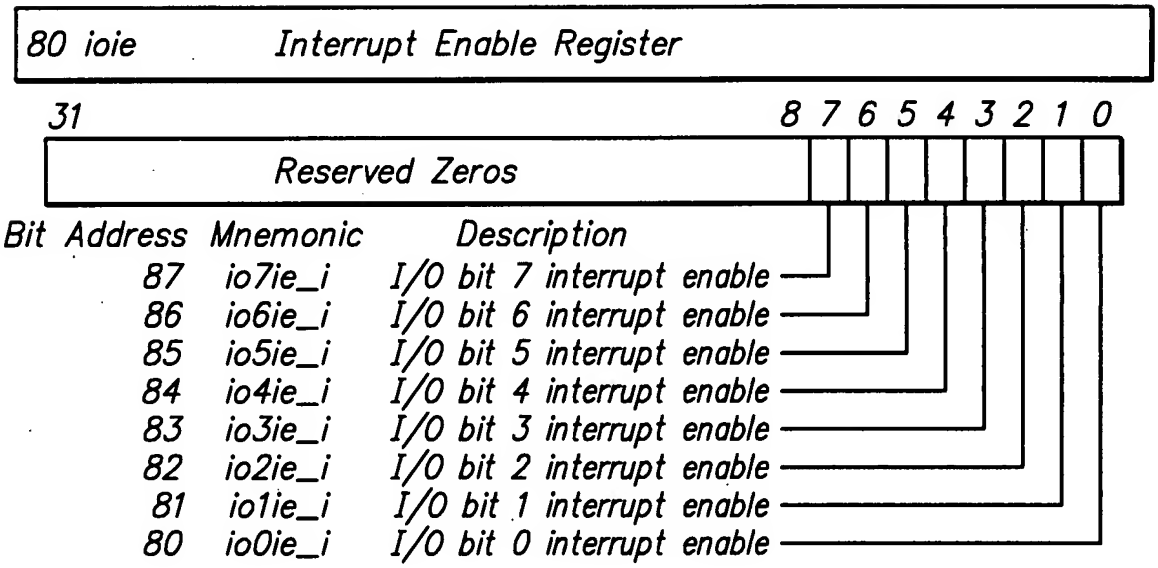

80 ioie Interrupt Enable Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Bit Address Mnemonic Description
87 io7ie_i I/O bit 7 interrupt enable
86 io6ie_i I/O bit 6 interrupt enable
85 io5ie_i I/O bit 5 interrupt enable
84 io4ie_i I/O bit 4 interrupt enable
83 io3ie_i I/O bit 3 interrupt enable
82 io2ie_i I/O bit 2 interrupt enable
81 io1ie_i I/O bit 1 interrupt enable
80 io0ie_i I/O bit 0 interrupt enable

FIG. 25

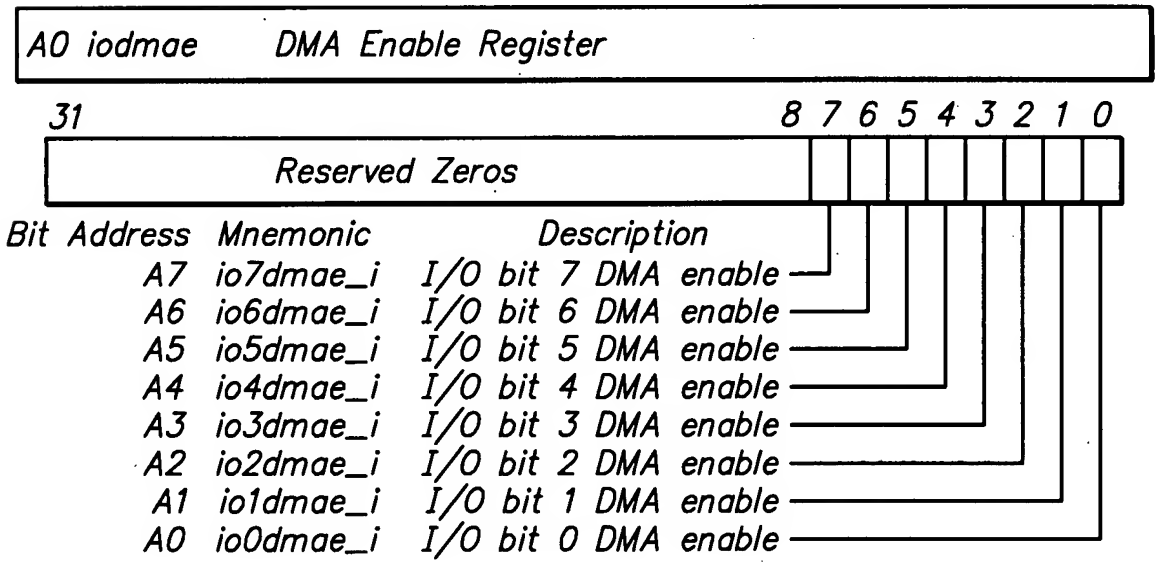

A0 iodmae DMA Enable Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Bit Address Mnemonic Description
A7 io7dmae_i I/O bit 7 DMA enable
A6 io6dmae_i I/O bit 6 DMA enable
A5 io5dmae_i I/O bit 5 DMA enable
A4 io4dmae_i I/O bit 4 DMA enable
A3 io3dmae_i I/O bit 3 DMA enable
A2 io2dmae_i I/O bit 2 DMA enable
A1 io1dmae_i I/O bit 1 DMA enable
A0 io0dmae_i I/O bit 0 DMA enable

FIG. 26

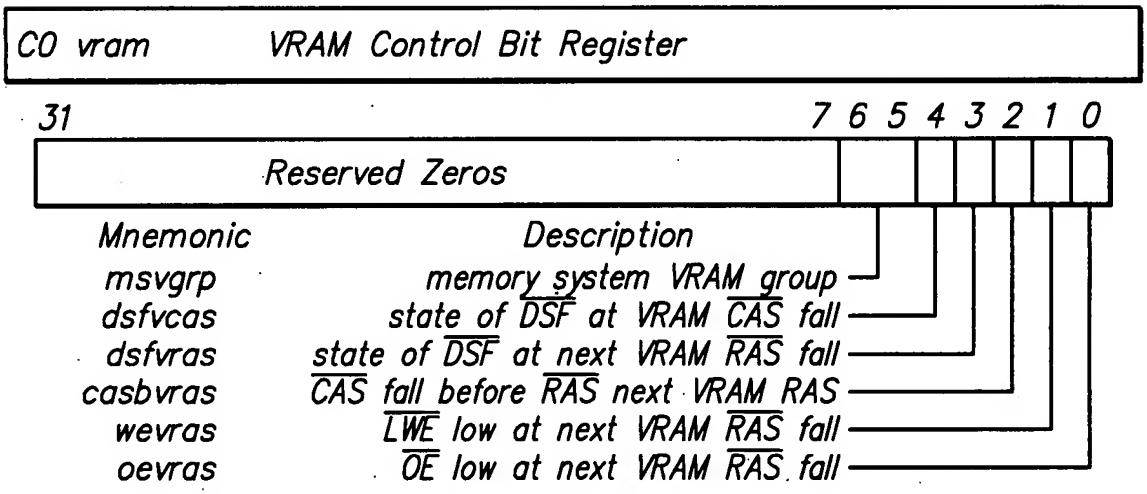

C0 vram VRAM Control Bit Register
31
7 6 5 4 3 2 1 0
Reserved Zeros
Mnemonic
Description
msvgrp
memory system VRAM group
dsfvcas
state of DSF at VRAM CAS fall
dsfvras
state of DSF at next VRAM RAS fall
casbvras
CAS fall before RAS next VRAM RAS
wevras
LWE low at next VRAM RAS fall
oevras
OE low at next VRAM RAS fall

FIG. 27

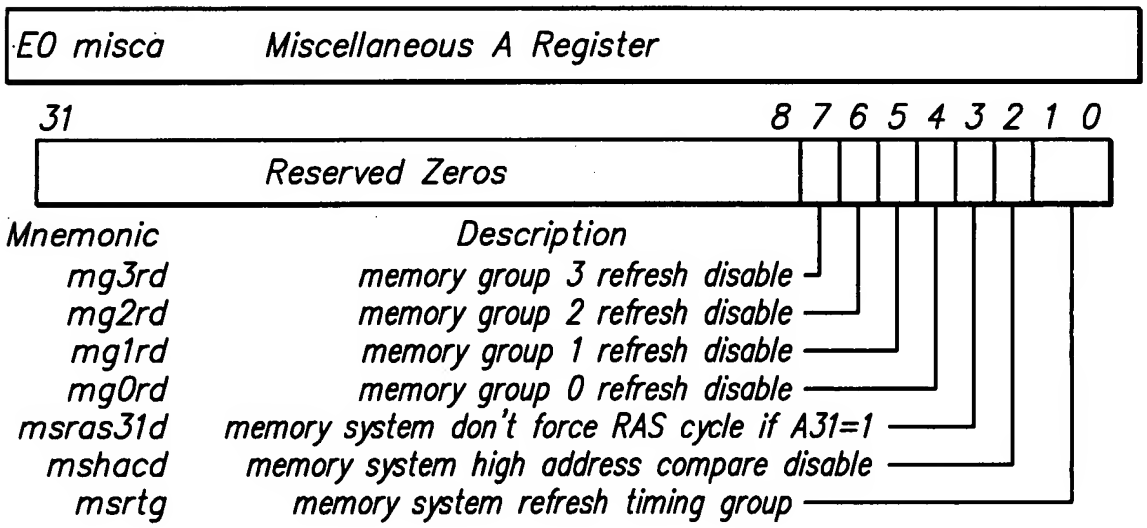

E0 misca Miscellaneous A Register
31
8 7 6 5 4 3 2 1 0
Reserved Zeros
Mnemonic
Description
mg3rd
memory group 3 refresh disable
mg2rd
memory group 2 refresh disable
mg1rd
memory group 1 refresh disable
mg0rd
memory group 0 refresh disable
msras31d
memory system don't force RAS cycle if A31=1
mshacd
memory system high address compare disable
msrtg
memory system refresh timing group

FIG. 28

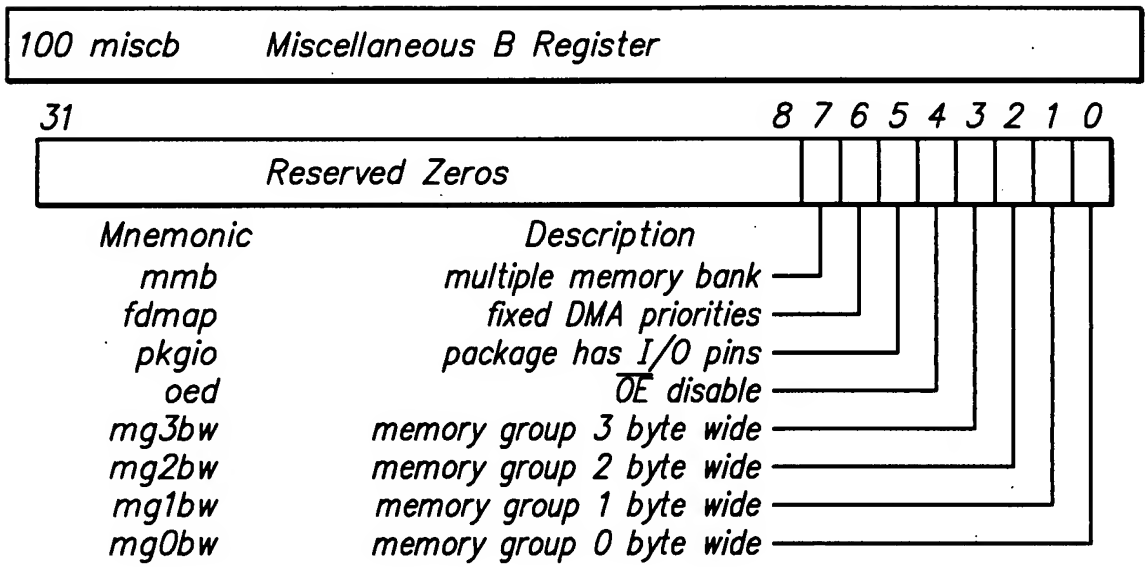
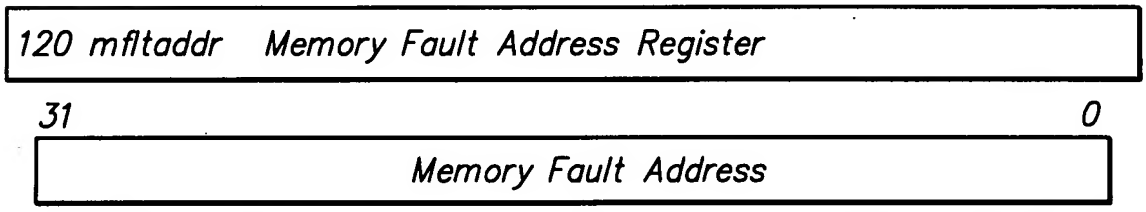
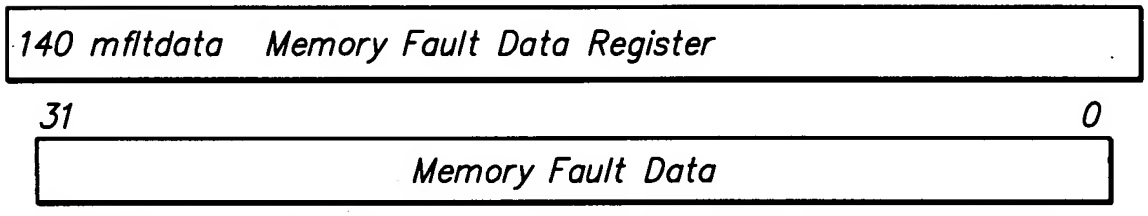


FIG. 29



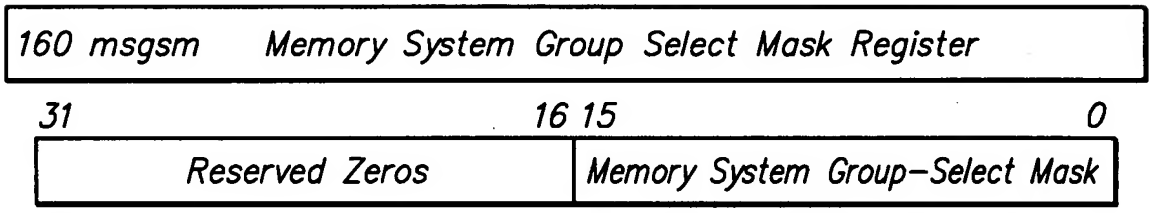
Register is read–only. Reading mfltaddr after a memory fault releases the data lock on mfltaddr and mfltdata, allowing data to flow into the registers.

FIG. 30



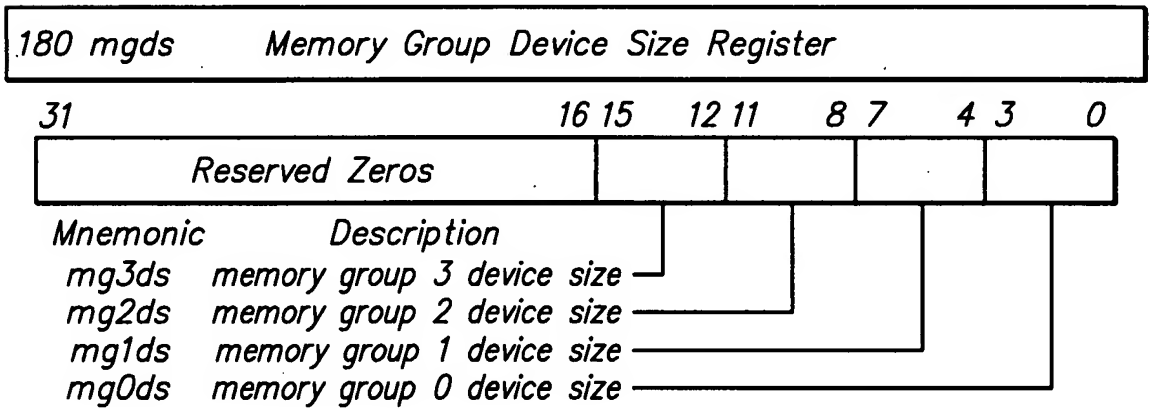
Register is read–only. Reading mfltaddr after a memory fault releases the data lock on mfltaddr and mfltdata, allowing data to flow into the registers.

FIG. 31



Contains zero, one, or two adjacent bits to determine which, if any, of the upper 16 address bits will be decoded to select memory groups.

FIG. 32



Device Sizes

0x00 64K DRAM	0x04 1M DRAM	0x08 8M DRAM	0x0c 64M DRAM (asym)
0x01 128K DRAM	0x05 2M DRAM	0x09 16M DRAM (asym)	0x0d 64M DRAM
0x02 256K DRAM	0x06 4M DRAM (asym)	0x0a 16M DRAM	0x0e 128M DRAM
0x03 512K DRAM	0x07 4M DRAM	0x0b 32M DRAM	0x0f SRAM

FIG. 33

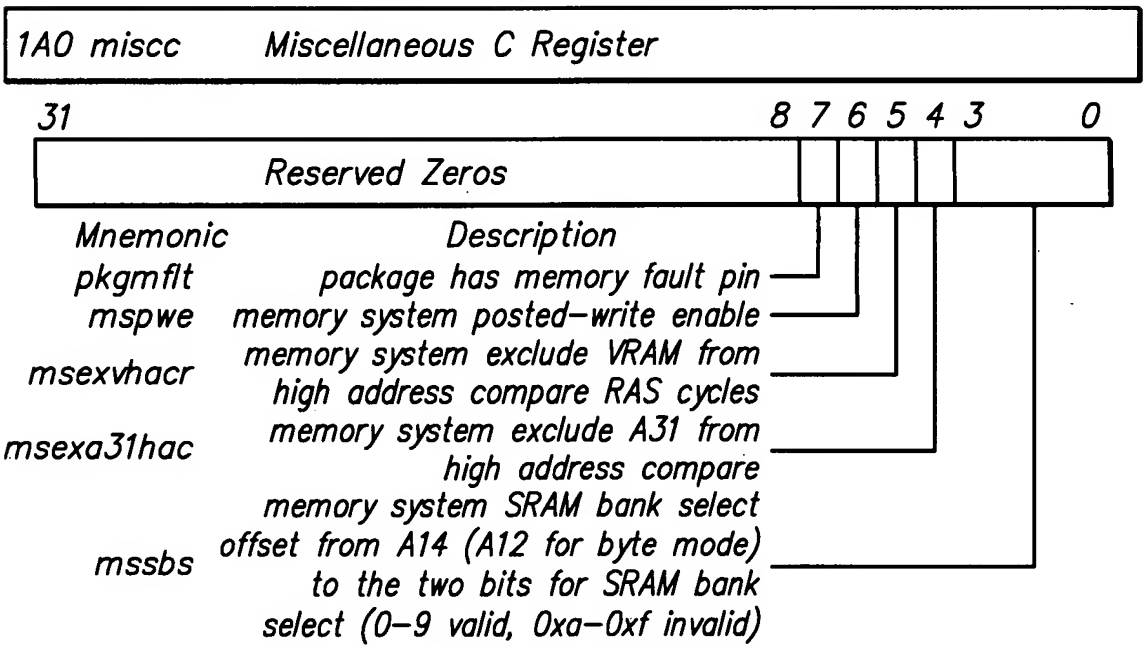

1A0 miscc Miscellaneous C Register
31
8 7 6 5 4 3 0
Reserved Zeros
Mnemonic
Description
pkgmflt
package has memory fault pin
mspwe
memory system posted-write enable
msexvhacr
memory system exclude VRAM from high address compare RAS cycles
msexa31hac
memory system exclude A31 from high address compare
mssbs
memory system SRAM bank select offset from A14 (A12 for byte mode) to the two bits for SRAM bank select (0-9 valid, 0xa-0xf invalid)

FIG. 34

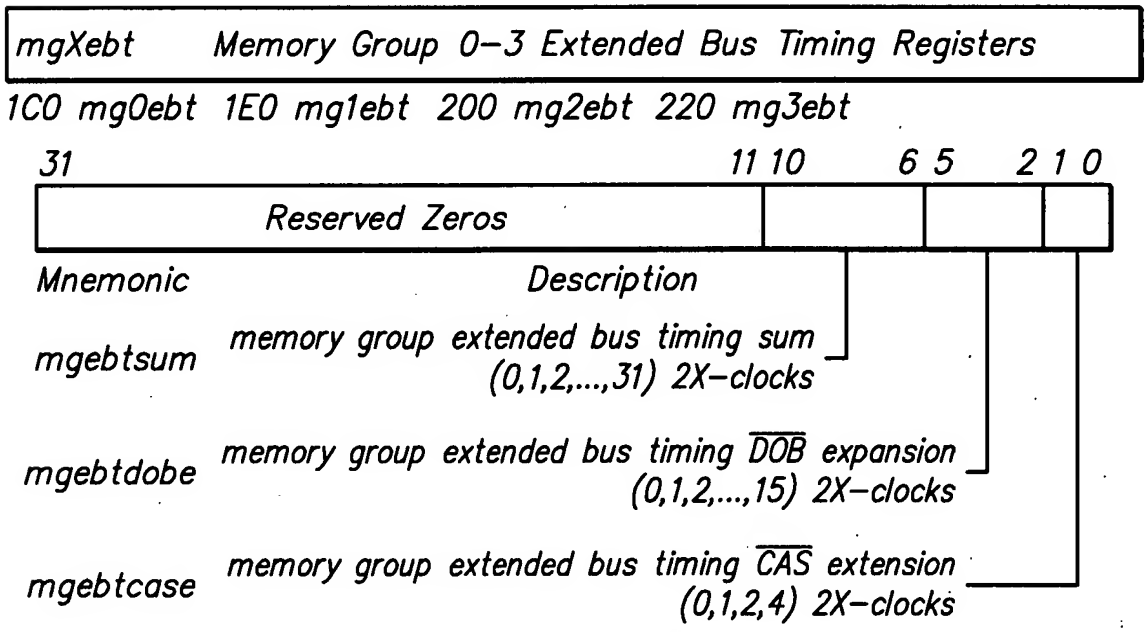

mgXebt Memory Group 0-3 Extended Bus Timing Registers
1C0 mg0ebt 1E0 mg1ebt 200 mg2ebt 220 mg3ebt
31
11 10 6 5 2 1 0
Reserved Zeros
Mnemonic
Description
mgebtsum
memory group extended bus timing sum (0,1,2,...,31) 2X-clocks
mgebtdobe
memory group extended bus timing DOB expansion (0,1,2,...,15) 2X-clocks
mgebtcase
memory group extended bus timing CAS extension (0,1,2,4) 2X-clocks

FIG. 35

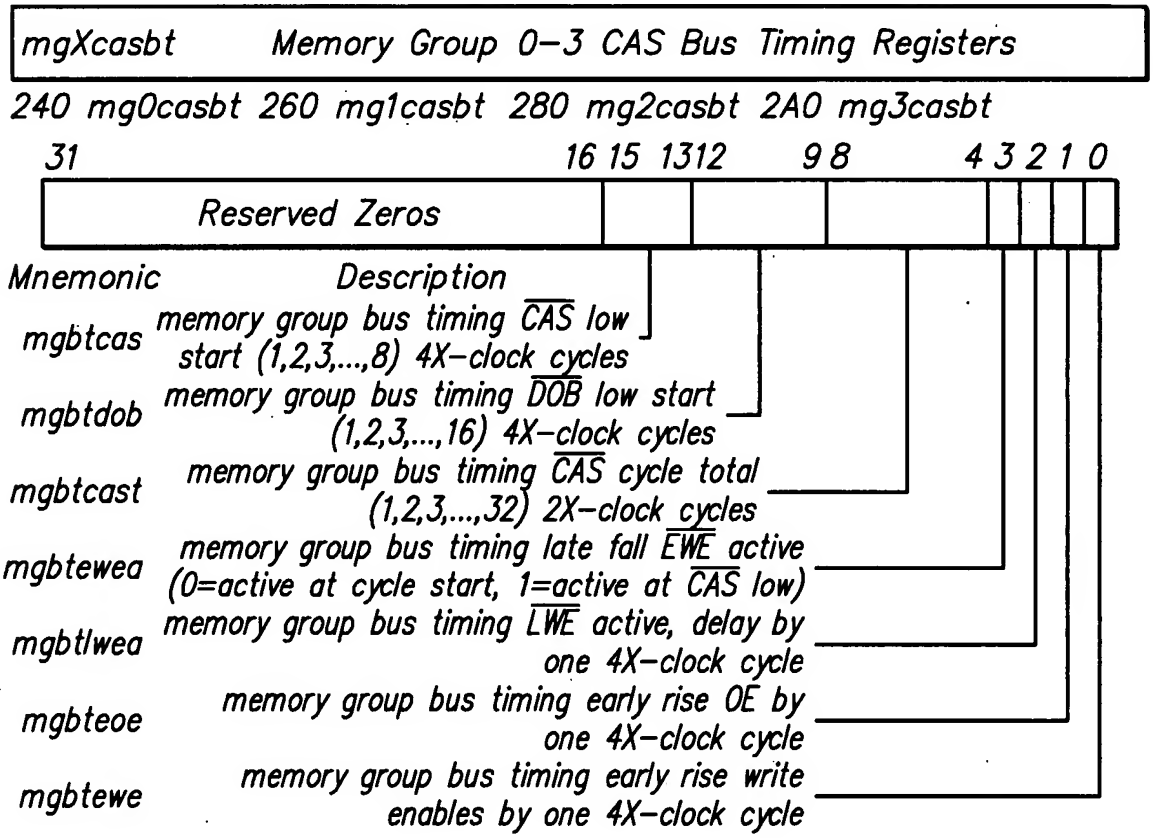

mgXcasbt Memory Group 0–3 CAS Bus Timing Registers
240 mg0casbt 260 mg1casbt 280 mg2casbt 2A0 mg3casbt
31
16 15 1312
9 8
4 3 2 1 0
Reserved Zeros
Mnemonic
Description
mgbtcas
memory group bus timing CAS low start (1,2,3,...,8) 4X–clock cycles
mgbtdob
memory group bus timing DOB low start (1,2,3,...,16) 4X–clock cycles
mgbtcast
memory group bus timing CAS cycle total (1,2,3,...,32) 2X–clock cycles
mgbtewea
memory group bus timing late fall EWE active (0=active at cycle start, 1=active at CAS low)
mgbtlwea
memory group bus timing LWE active, delay by one 4X–clock cycle
mgbteoe
memory group bus timing early rise OE by one 4X–clock cycle
mgbtewe
memory group bus timing early rise write enables by one 4X–clock cycle

FIG. 36

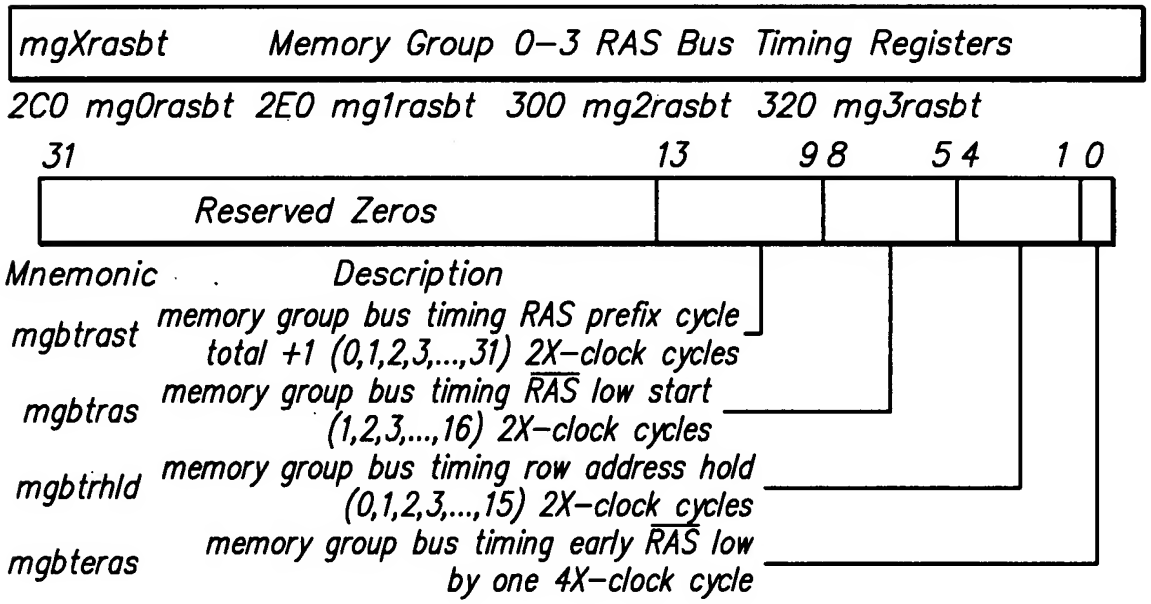

mgXrasbt Memory Group 0–3 RAS Bus Timing Registers
2C0 mg0rasbt 2E0 mg1rasbt 300 mg2rasbt 320 mg3rasbt
31
13
9 8
5 4
1 0
Reserved Zeros
Mnemonic
Description
mgbtrast
memory group bus timing RAS prefix cycle total +1 (0,1,2,3,...,31) 2X–clock cycles
mgbtras
memory group bus timing RAS low start (1,2,3,...,16) 2X–clock cycles
mgbtrhld
memory group bus timing row address hold (0,1,2,3,...,15) 2X–clock cycles
mgbteras
memory group bus timing early RAS low by one 4X–clock cycle

FIG. 37

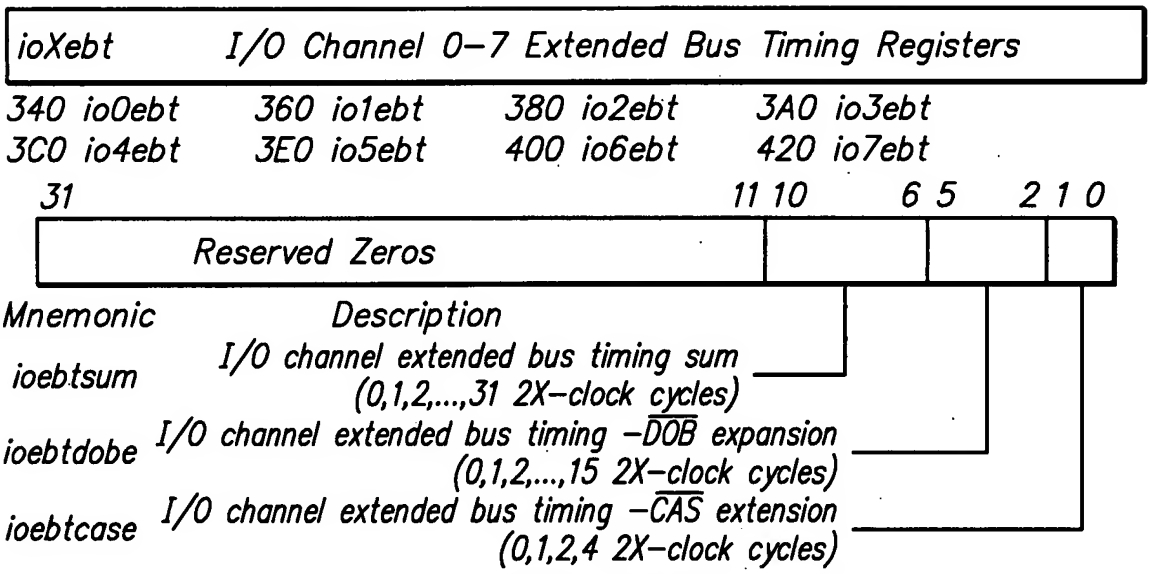


FIG. 38

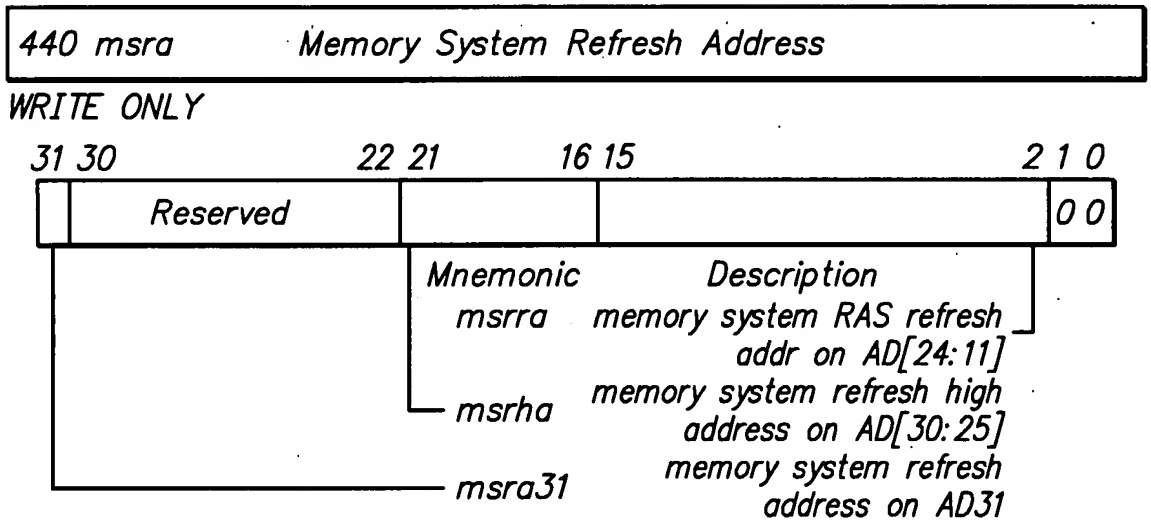


FIG. 39

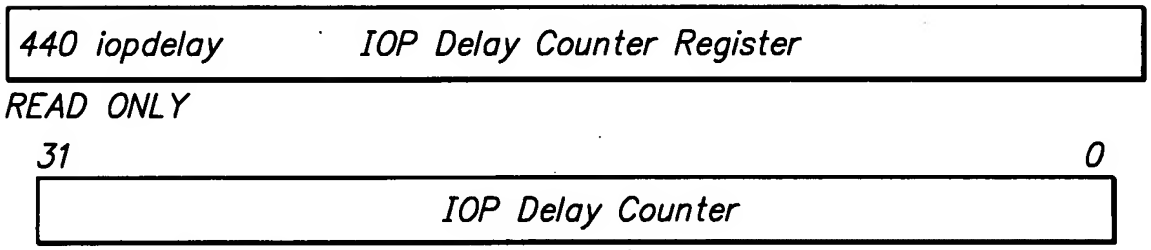


FIG. 40

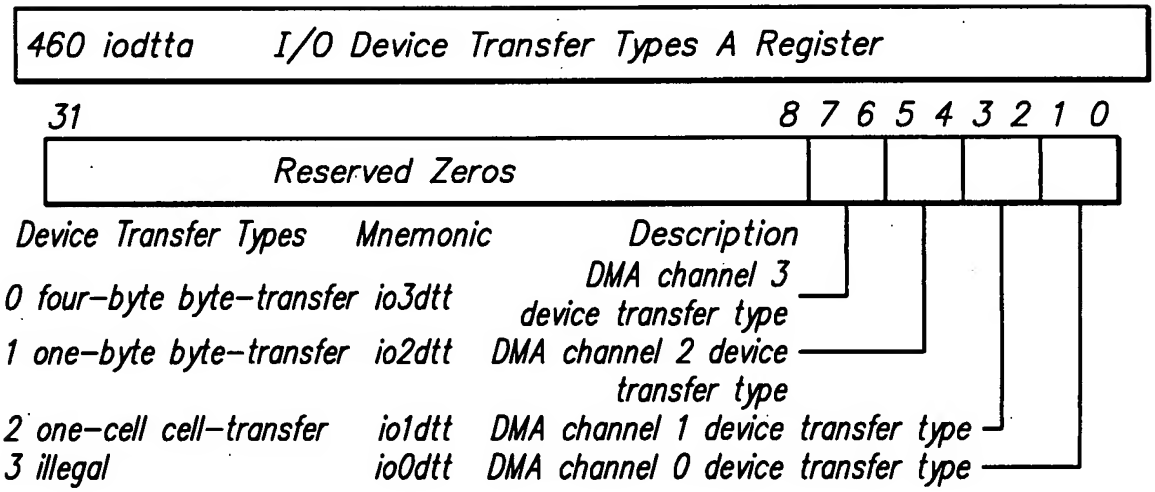


FIG. 41

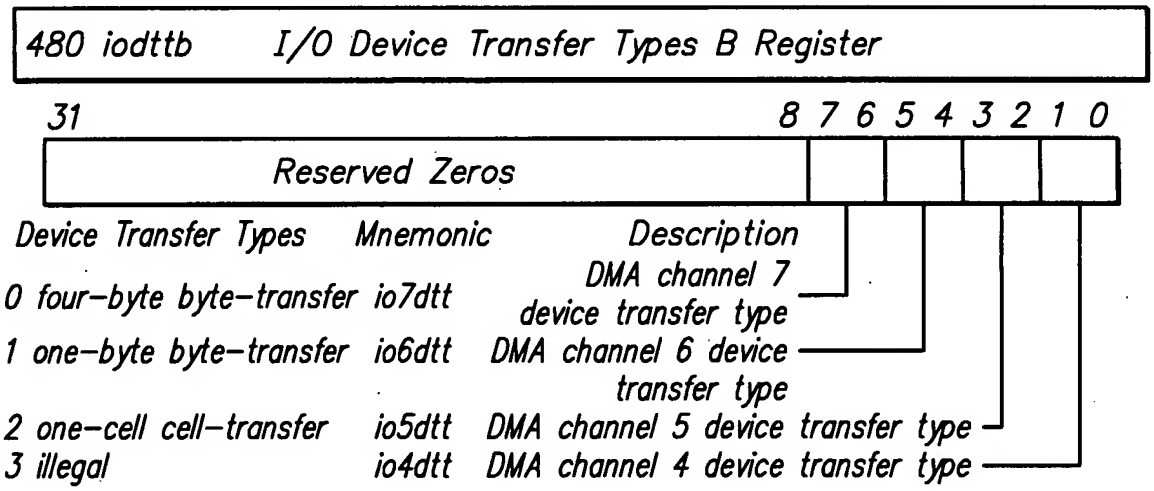


FIG. 42

FIG. 43

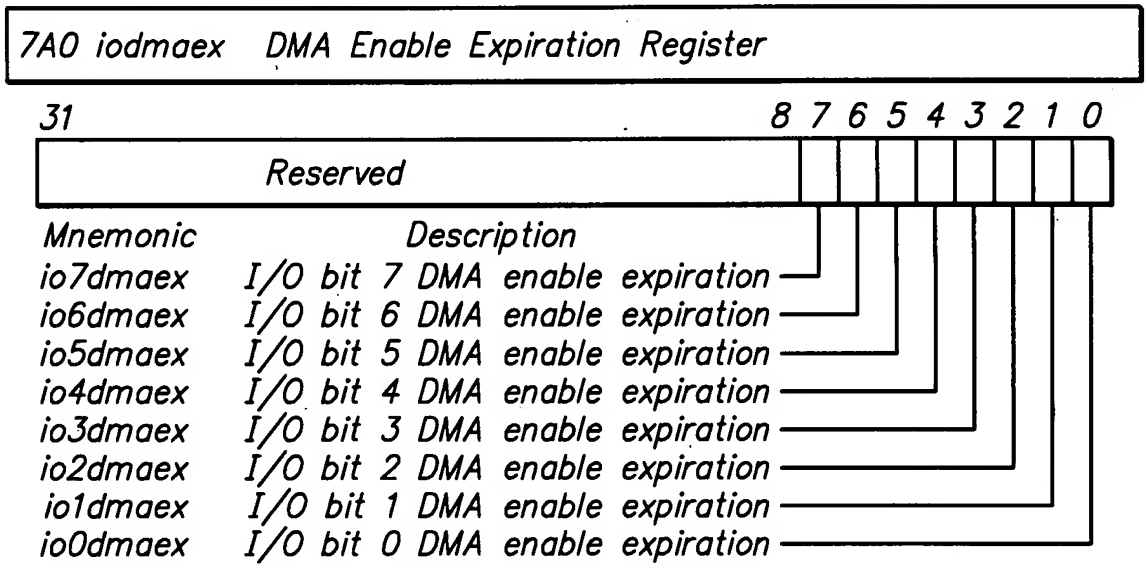


FIG. 44

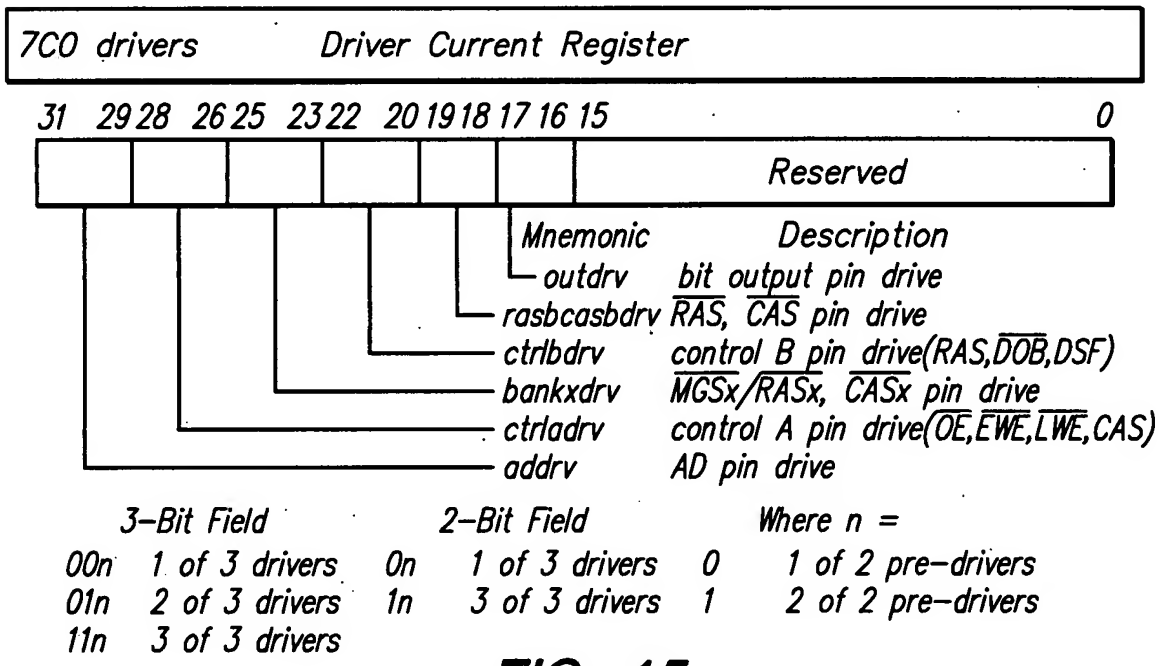


FIG. 45

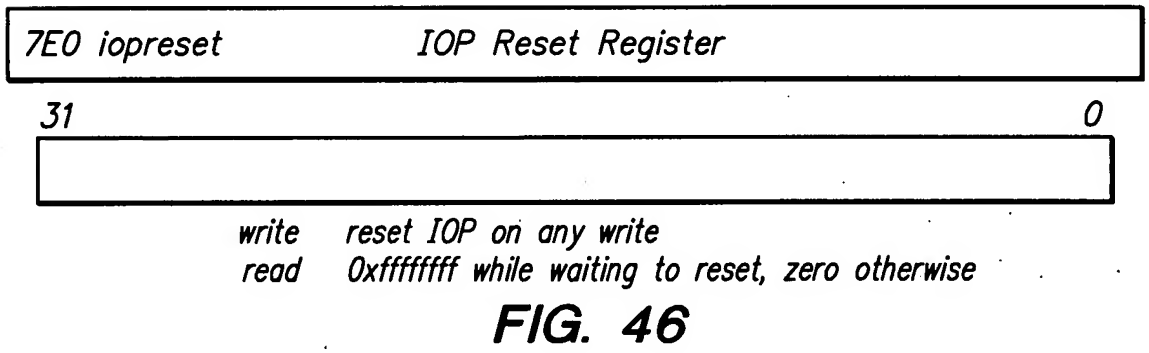


FIG. 46

27/57

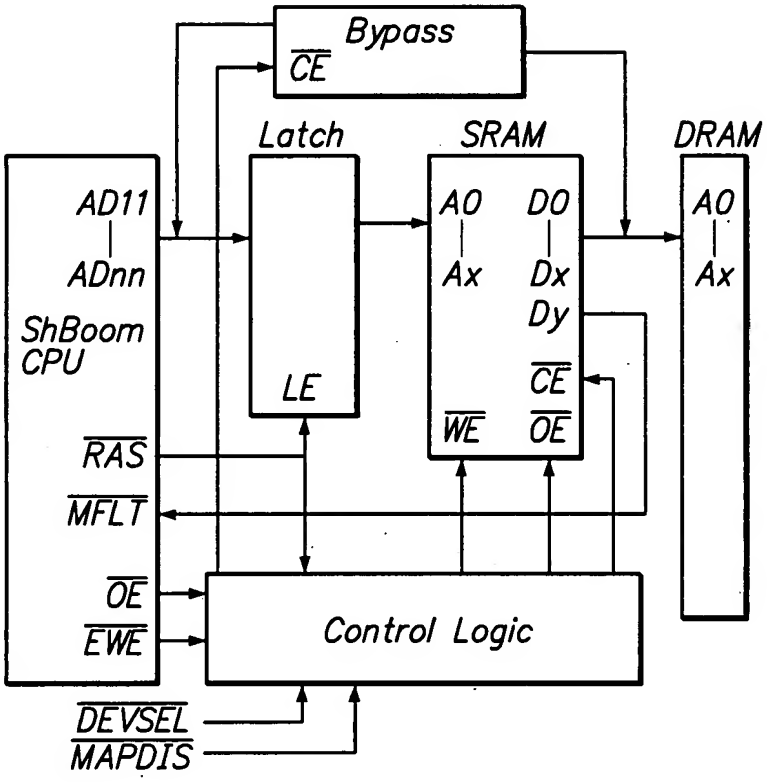

Bypass
CE
Latch
SRAM
DRAM
AD11
ADnn
ShBoom
CPU
LE
A0
Ax
D0
Dx
Dy
CE
WE
OE
A0
Ax
RAS
MFLT
OE
EWE
Control Logic
DEVSEL
MAPDIS

FIG. 46A

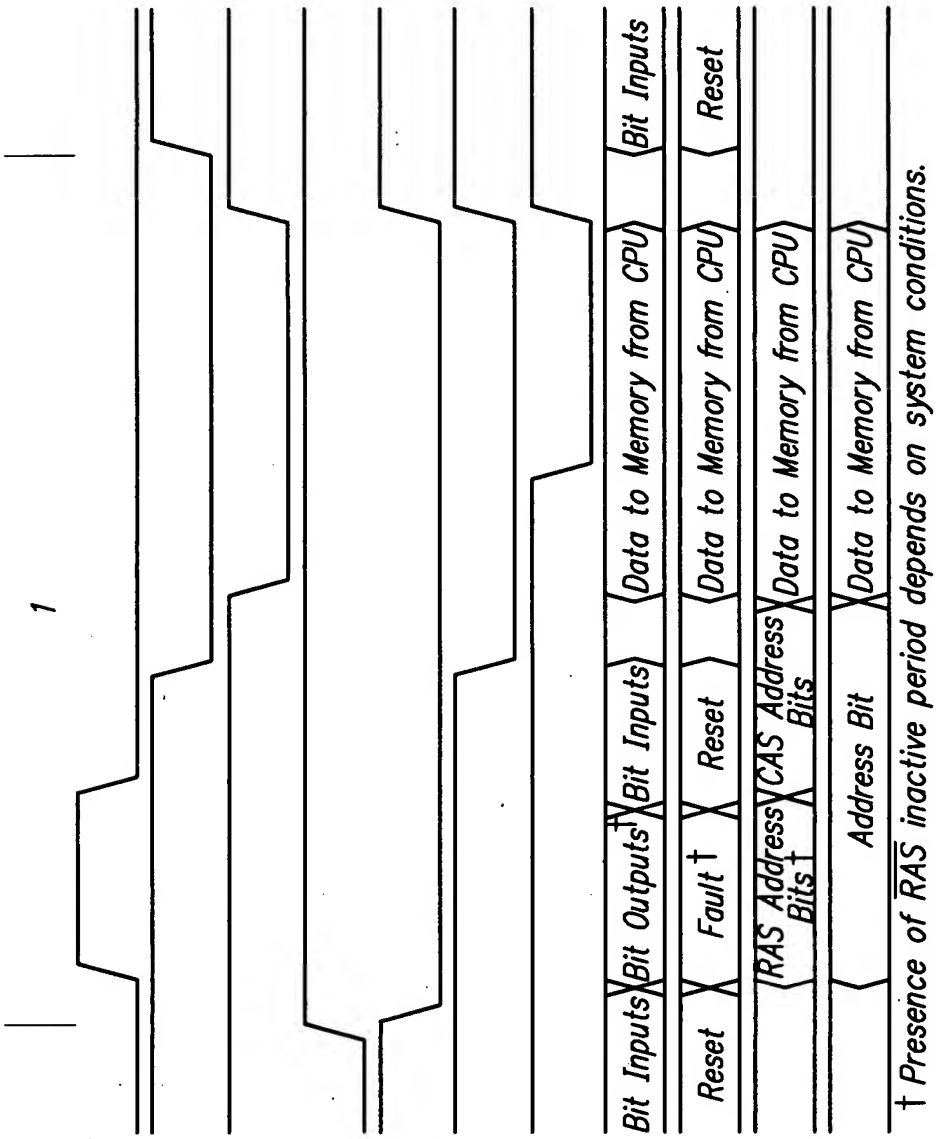

1
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs
Bit Inputs
Data to Memory from CPU
Reset
Fault †
Reset
Data to Memory from CPU
RAS Address Bits †
CAS Address Bits
Data to Memory from CPU
Address Bit
Data to Memory from CPU
Reset
† Presence of RAS inactive period depends on system conditions.

FIG. 47

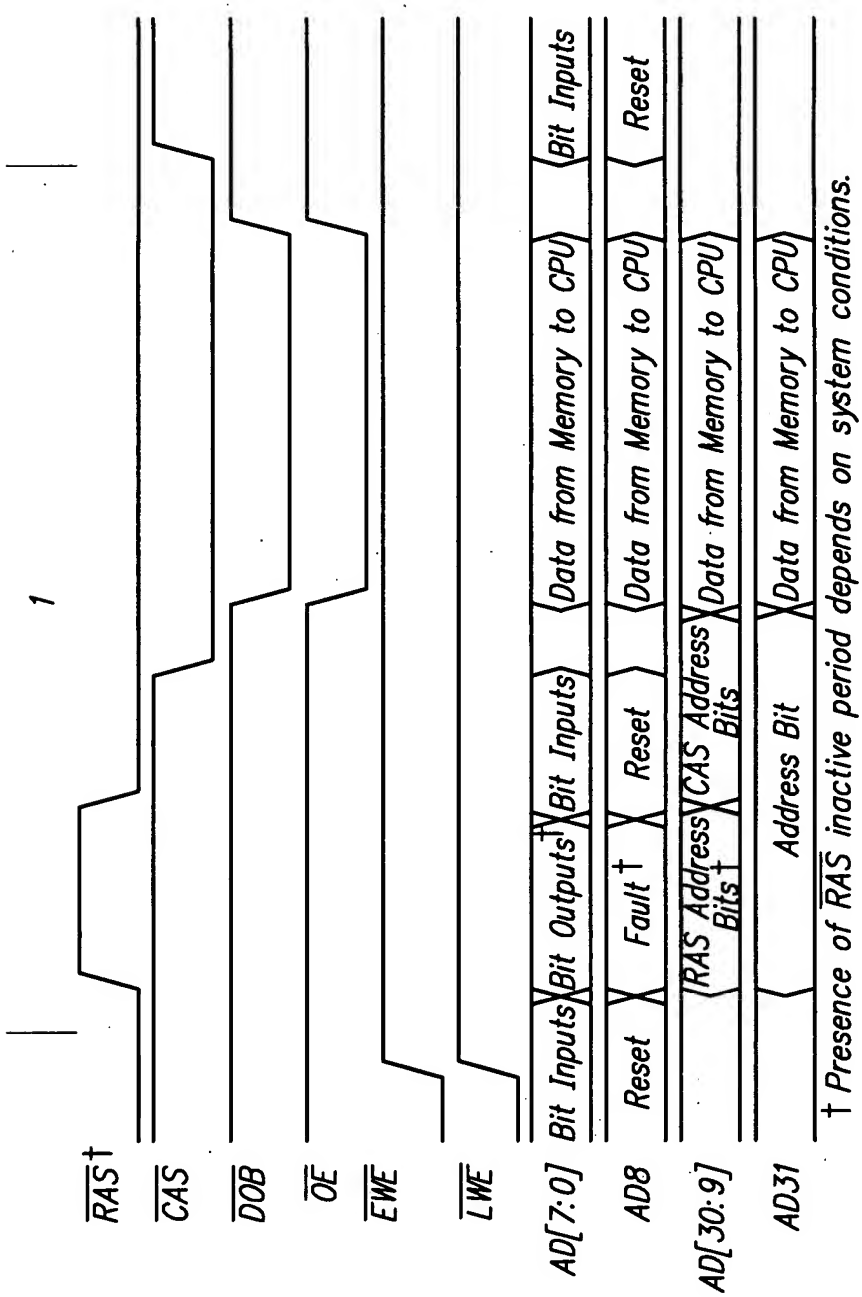

1
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs†
Data from Memory to CPU
Reset
Fault†
RAS Address Bits†
CAS Address Bits
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 48

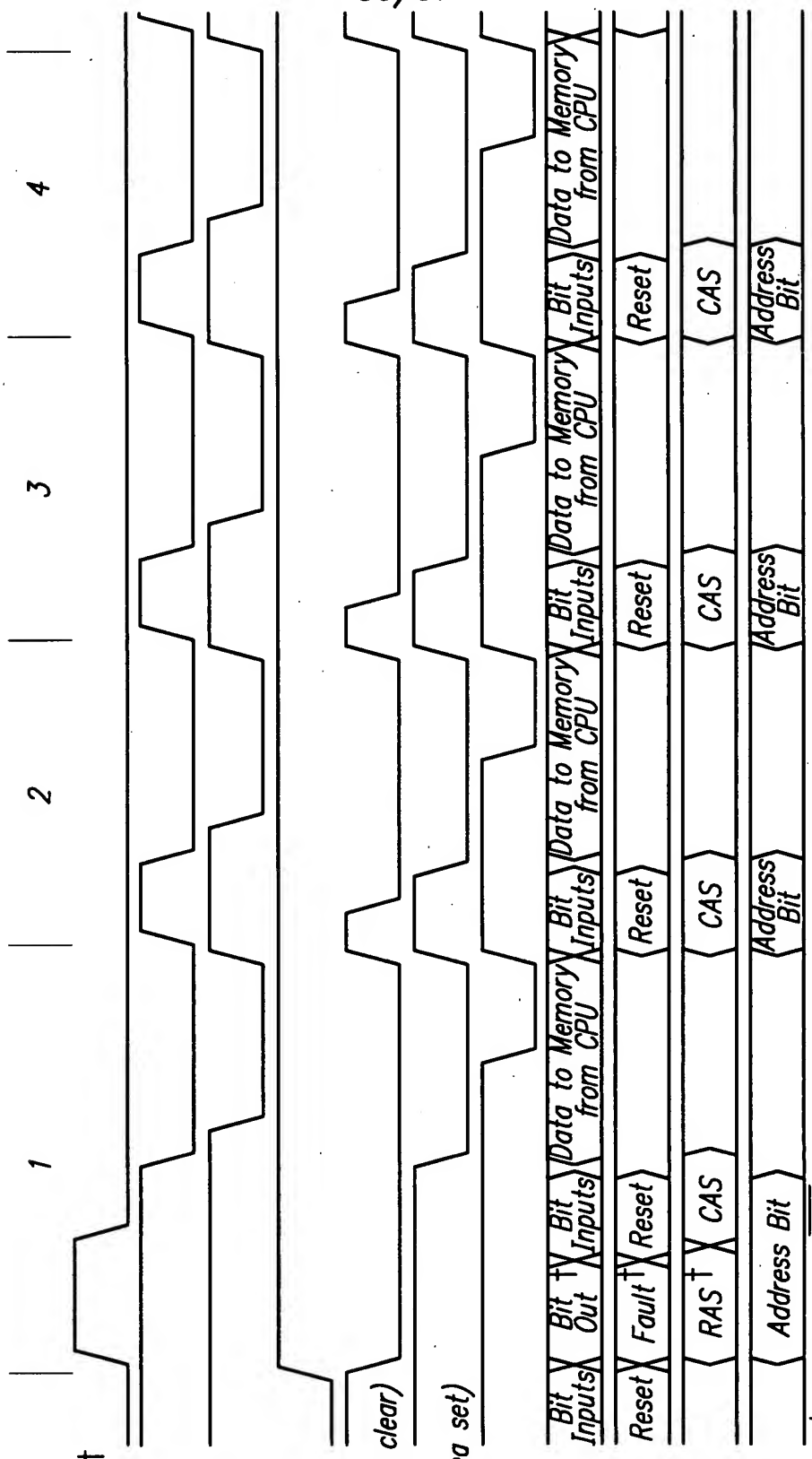

1
2
3
4
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out †
Data to Memory from CPU
Reset
Fault †
RAS †
CAS
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 49

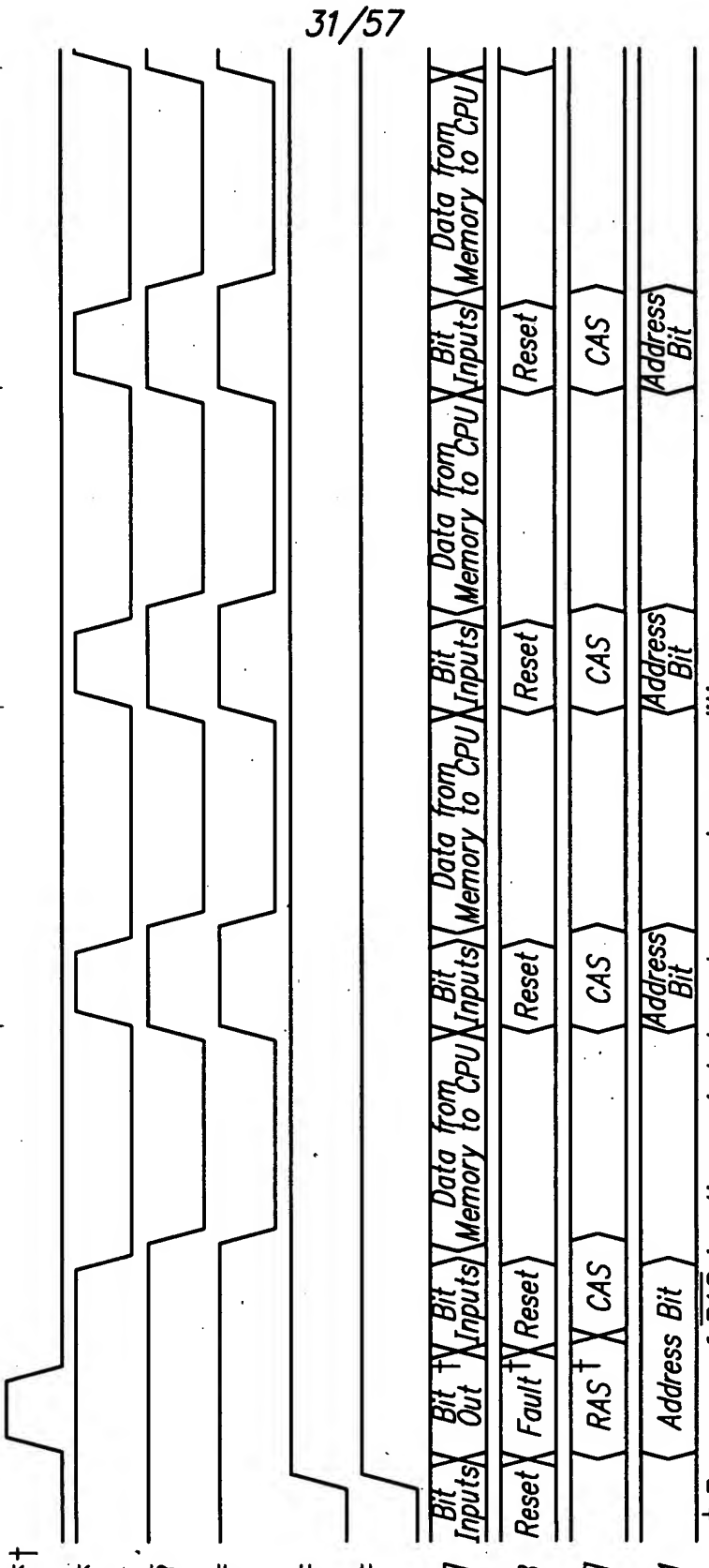

1
2
3
4
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out
Data from Memory to CPU
Reset
Fault†
RAS†
CAS
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 50

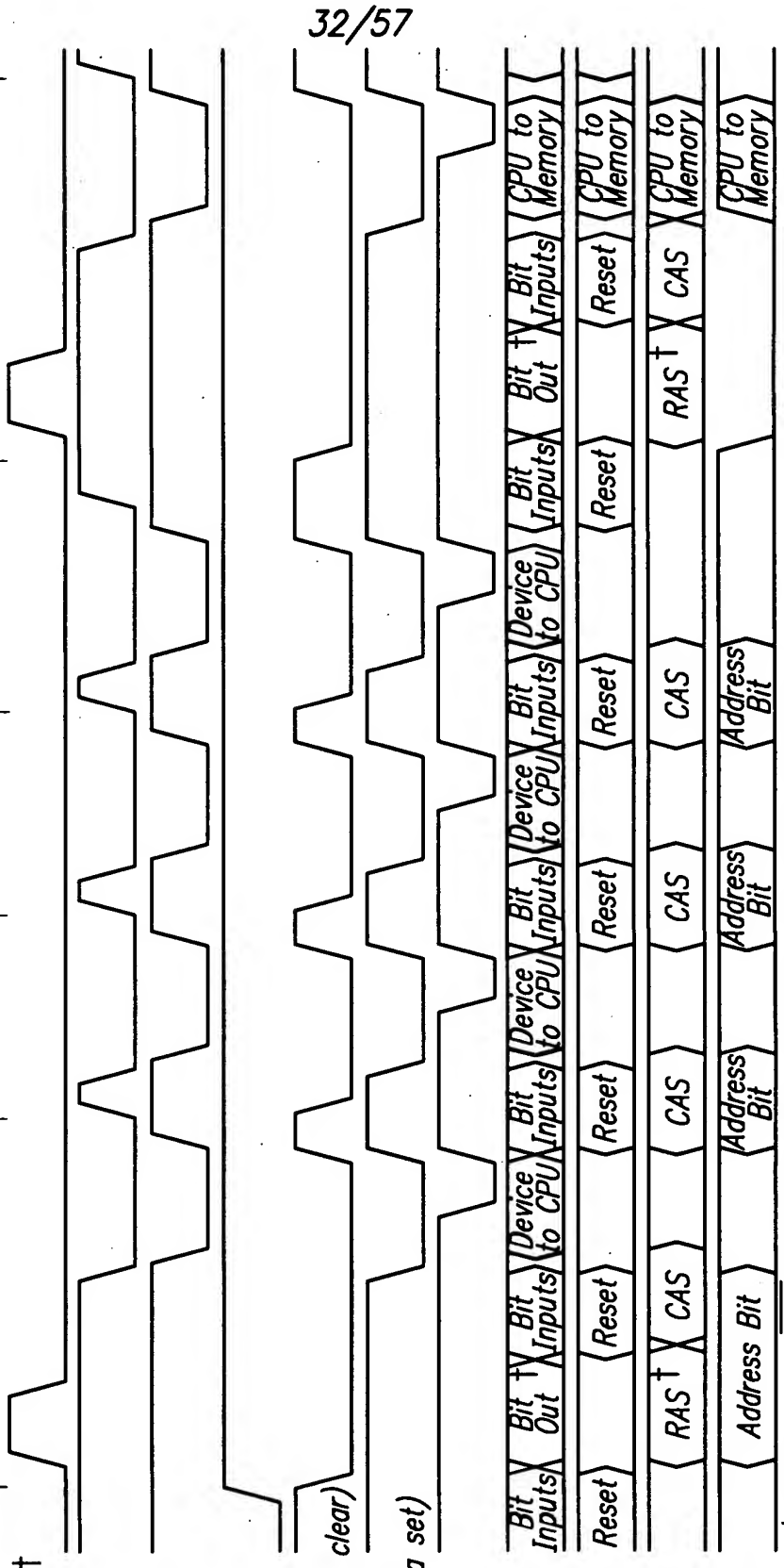

1
2
3
4
5
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out †
Device to CPU
Reset
CAS
RAS †
Address Bit
CPU to Memory
† Presence of RAS inactive period depends on system conditions.

FIG. 51

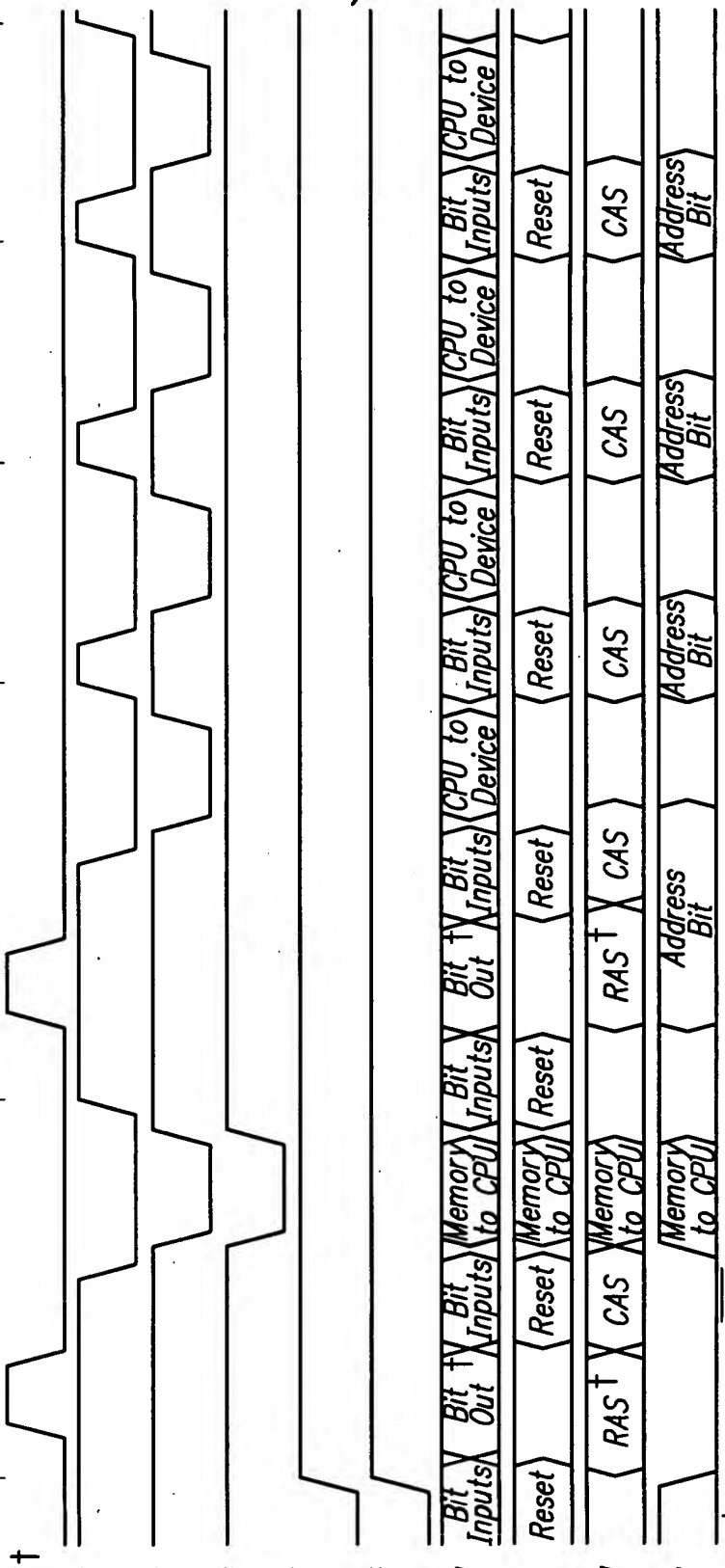

1
2
3
4
5
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out †
Memory to CPU
CPU to Device
Reset
RAS †
CAS
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 52

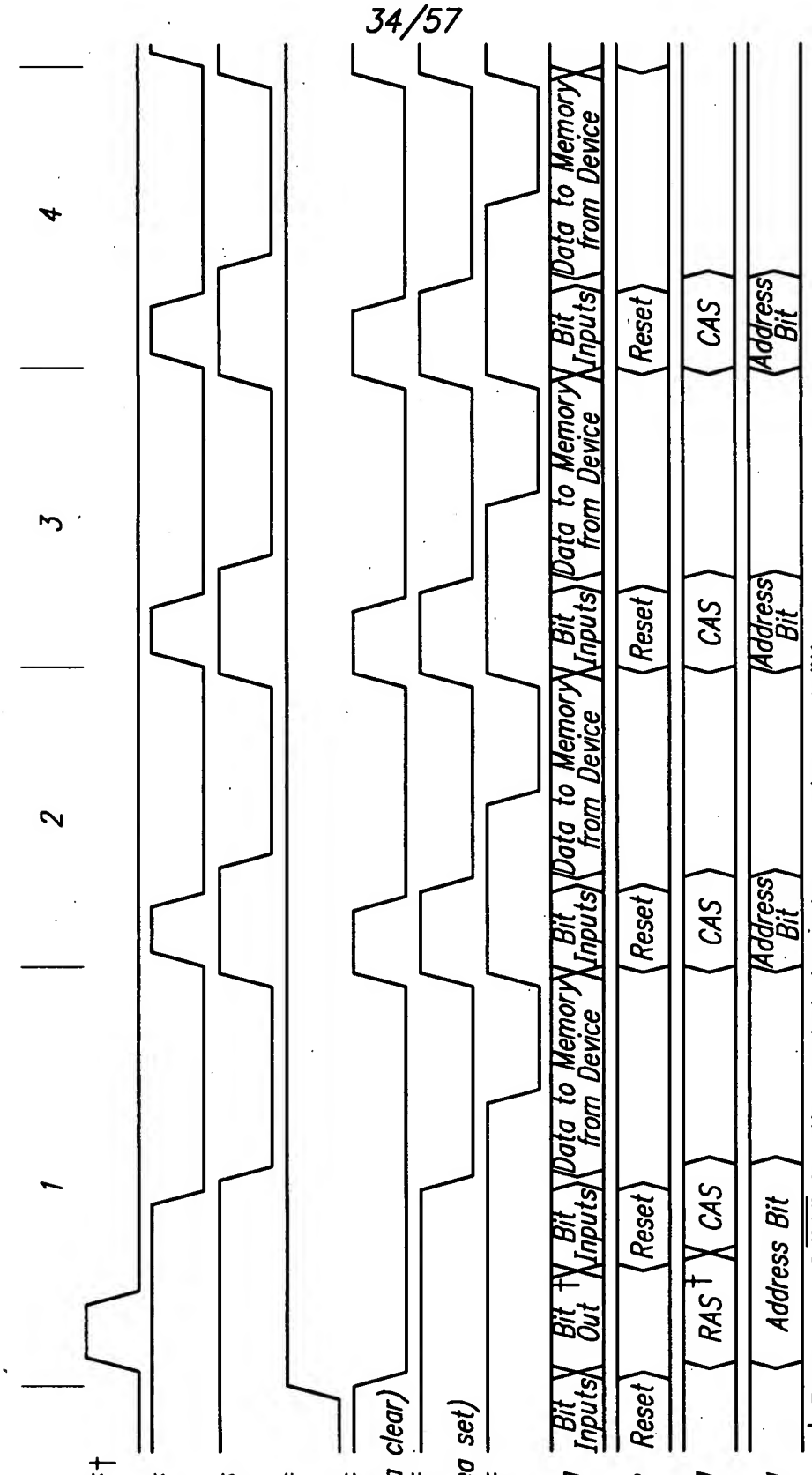

1
2
3
4
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out †
Data to Memory from Device
Reset
RAS †
CAS
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 53

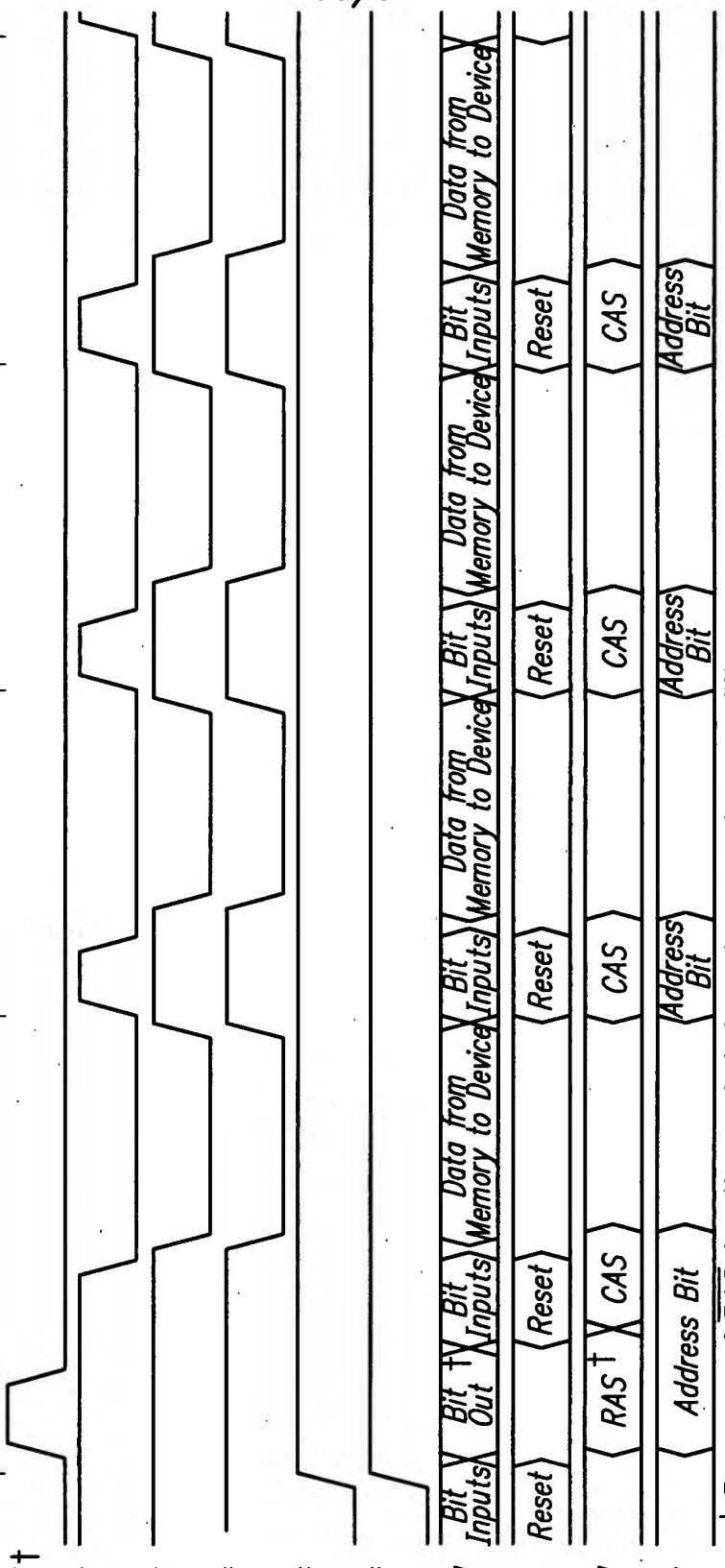

1
2
3
4
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit † Out
Data from Memory to Device
Reset
RAS †
CAS
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 54

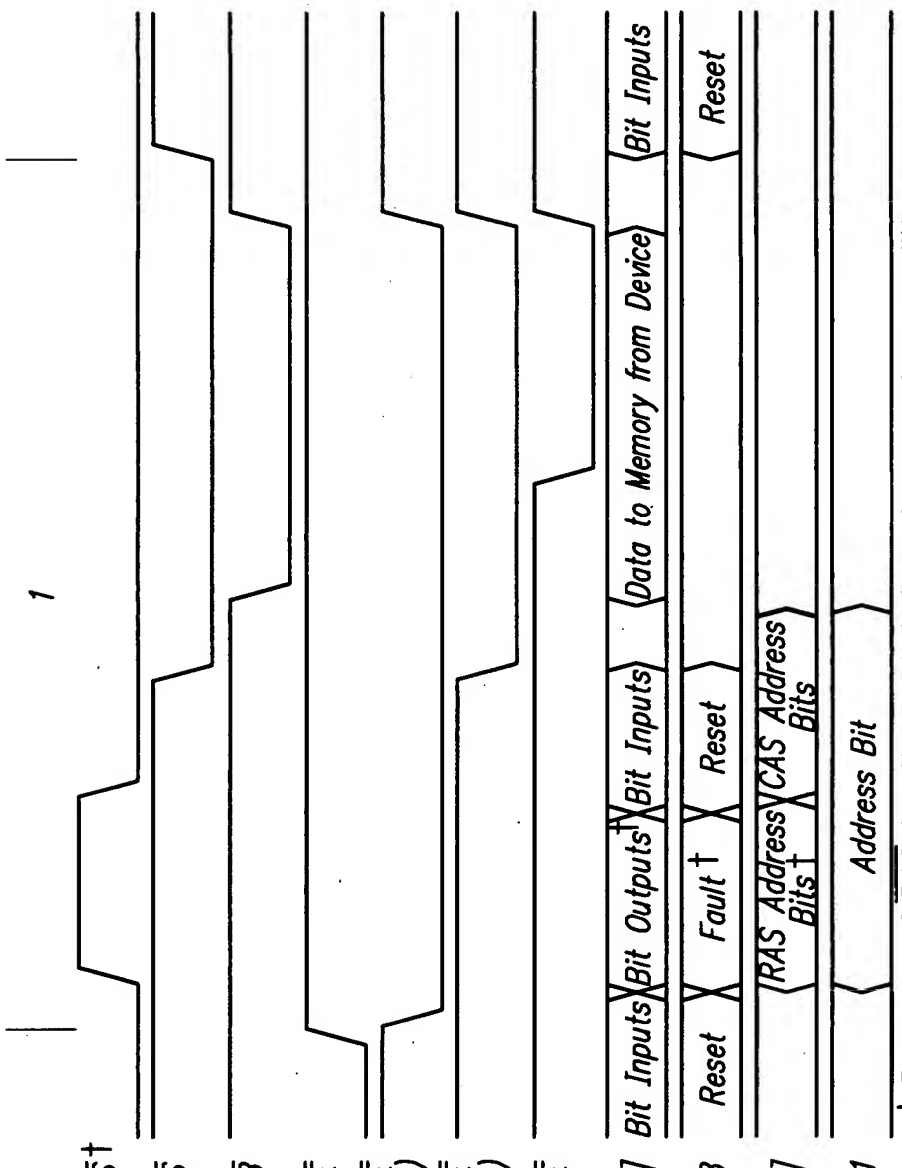

1
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs†
Bit Inputs
Data to Memory from Device
Bit Inputs
Reset
Fault†
Reset
Reset
RAS Address Bits†
CAS Address Bits
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 55

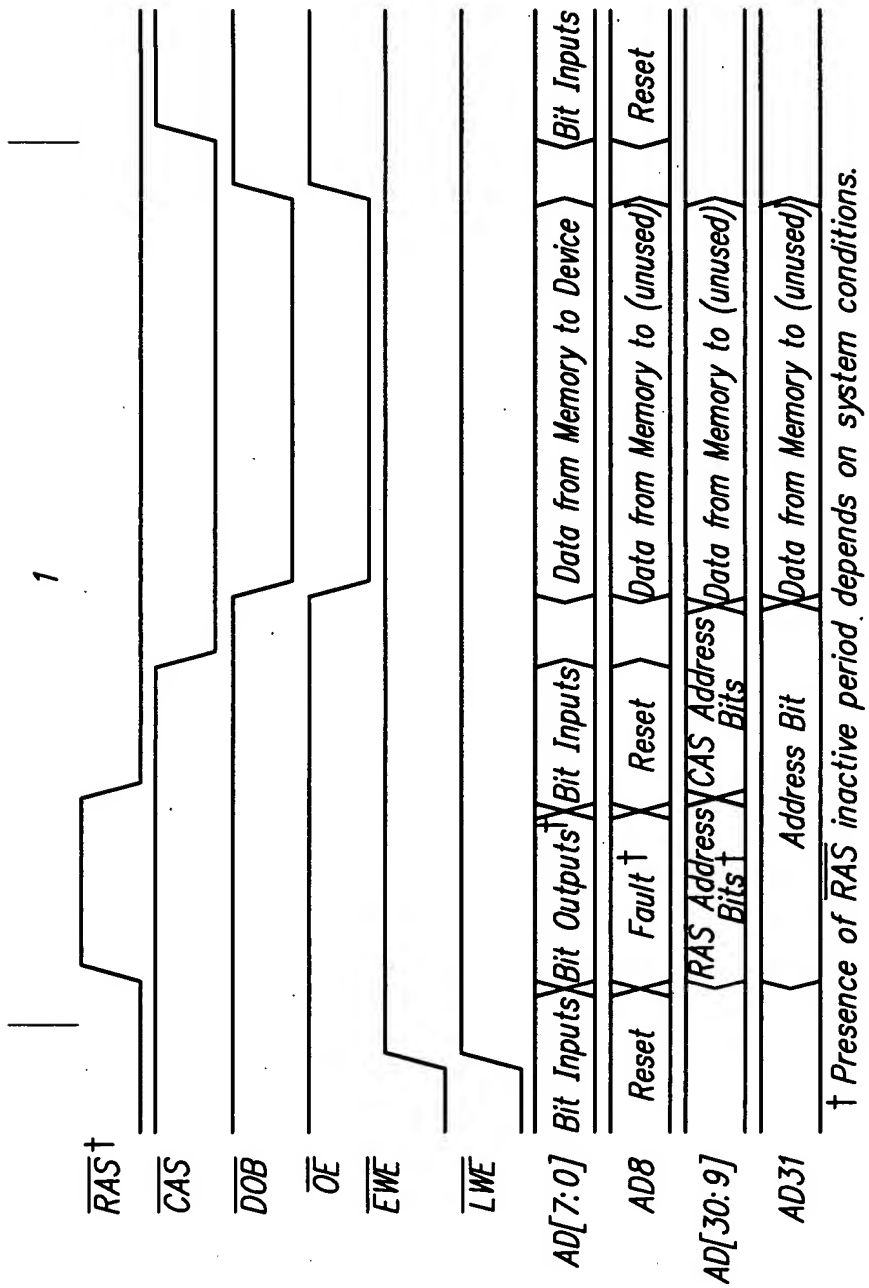

1
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs†
Bit Inputs
Data from Memory to Device
Bit Inputs
Reset
Fault†
Reset
Data from Memory to (unused)
Reset
RAS Address Bits†
CAS Address Bits
Data from Memory to (unused)
Address Bit
Data from Memory to (unused)
† Presence of RAS inactive period depends on system conditions.

FIG. 56

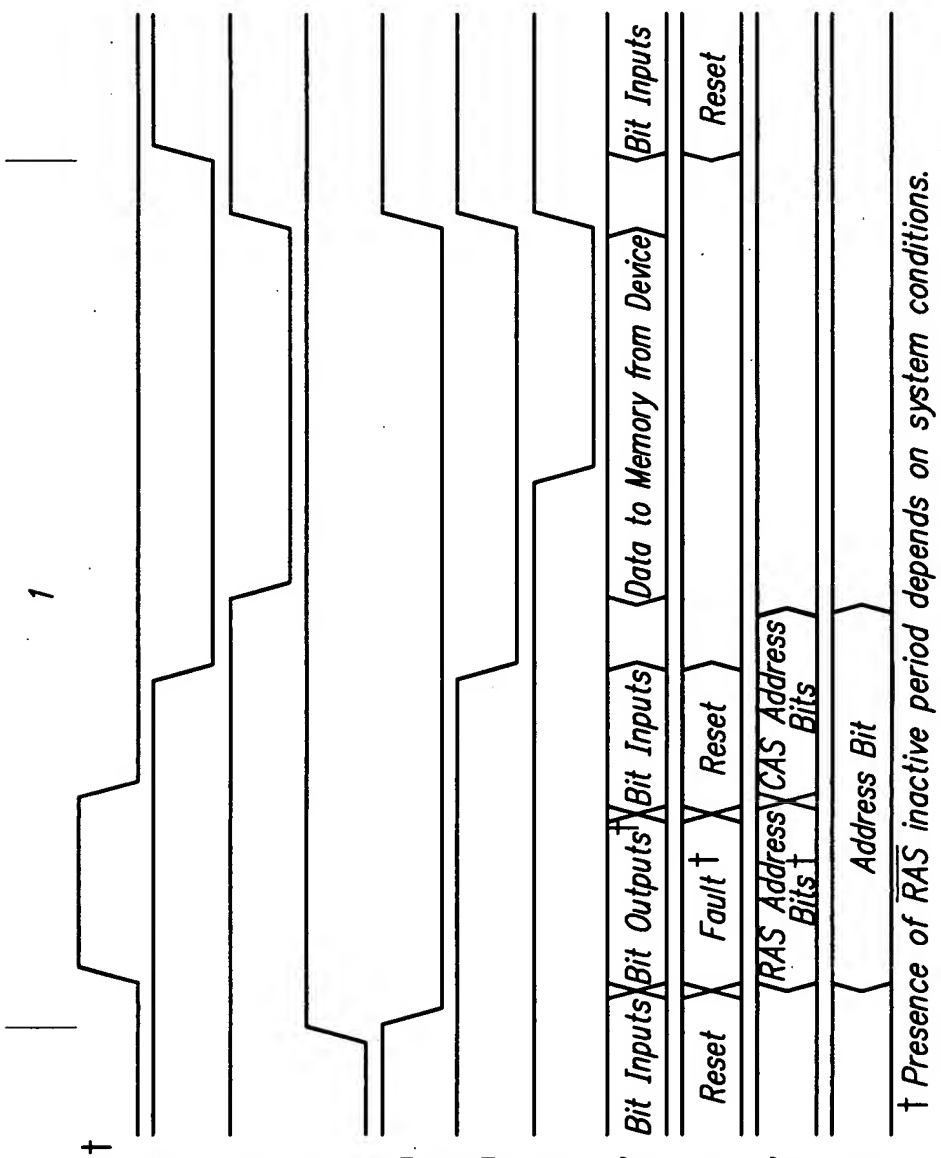

1
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs†
Bit Inputs
Data to Memory from Device
Bit Inputs
Reset
Fault†
Reset
Reset
RAS Address Bits†
CAS Address Bits
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 57

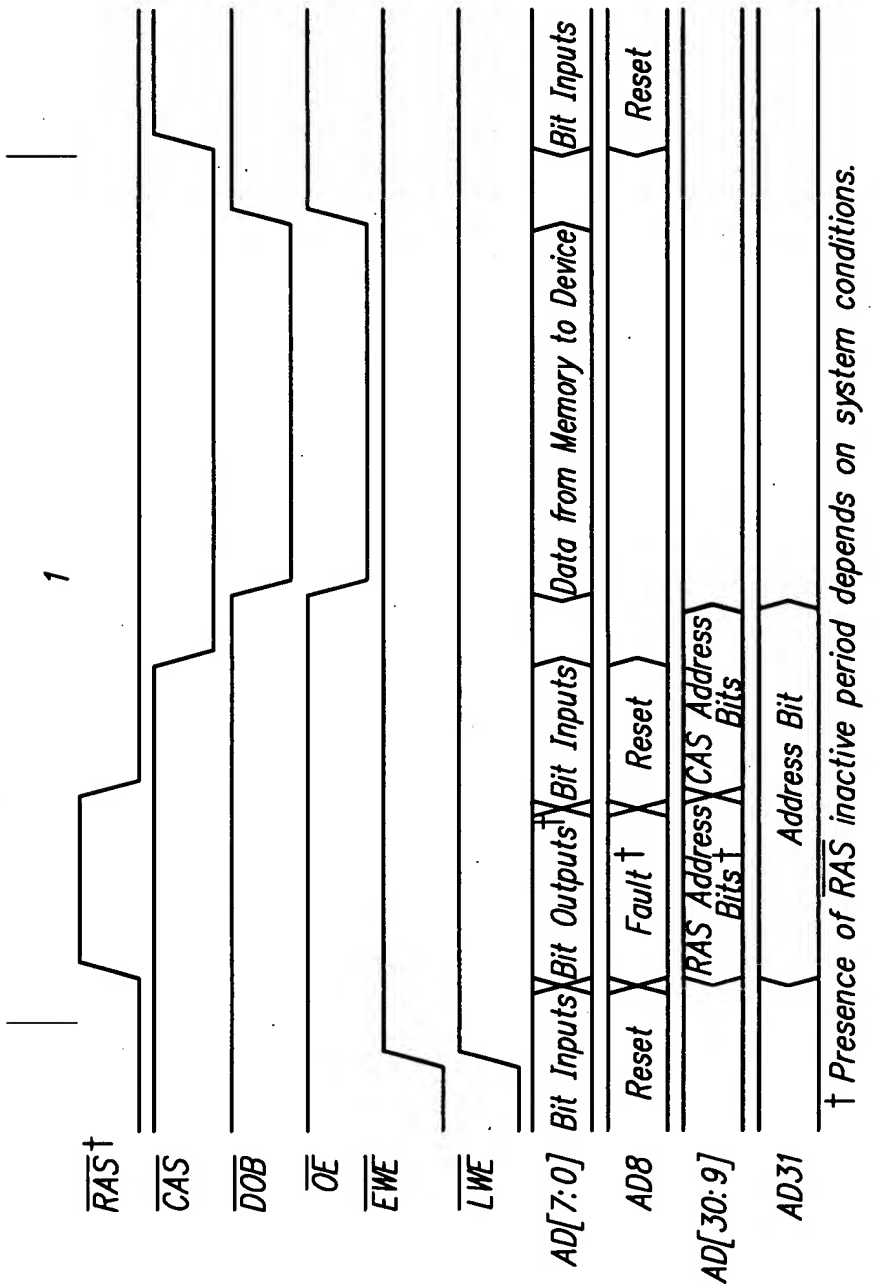

1
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs††
Bit Inputs
Data from Memory to Device
Bit Inputs
Reset
Fault †
Reset
Reset
RAS Address Bits †
CAS Address Bits
Address Bit
† Presence of RAS inactive period depends on system conditions.

FIG. 58

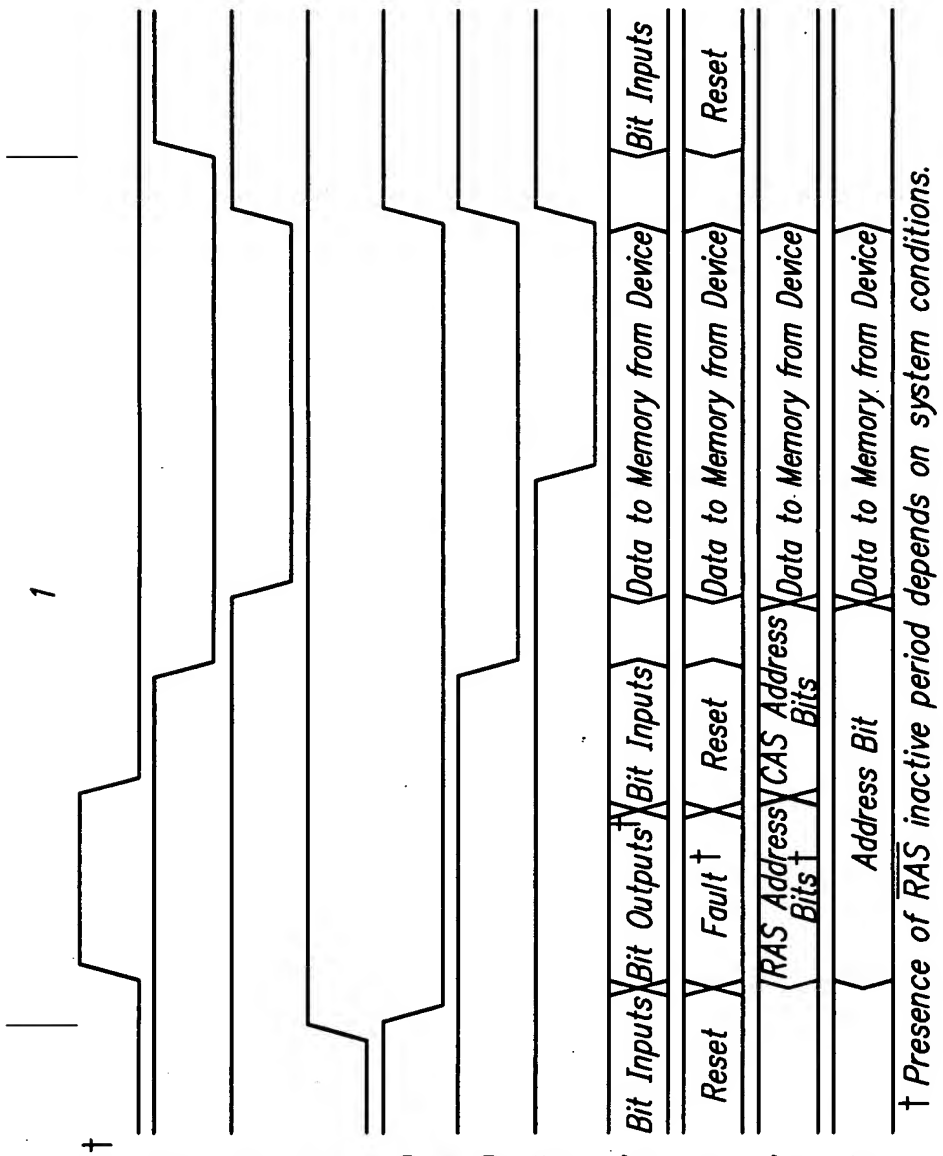

1
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs†
Bit Inputs
Data to Memory from Device
Reset
Fault†
Reset
Data to Memory from Device
RAS Address Bits†
CAS Address Bits
Data to Memory from Device
Address Bit
Data to Memory from Device
Reset
† Presence of RAS inactive period depends on system conditions.

FIG. 59

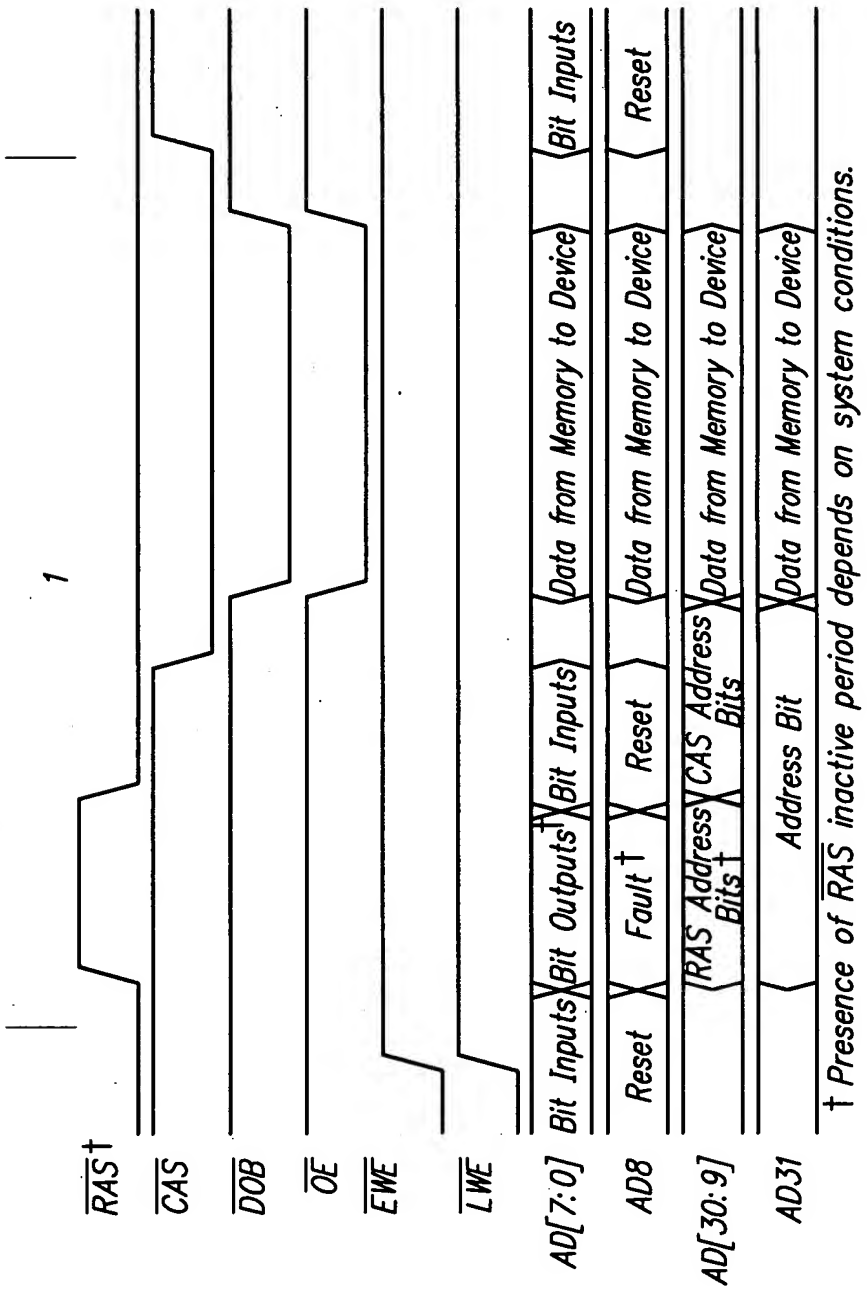

1
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Outputs††
Bit Inputs
Reset
Fault †
Reset
RAS Address Bits †
CAS Address Bits
Address Bit
Data from Memory to Device
Data from Memory to Device
Data from Memory to Device
Data from Memory to Device
Bit Inputs
Reset
† Presence of RAS inactive period depends on system conditions.

FIG. 60

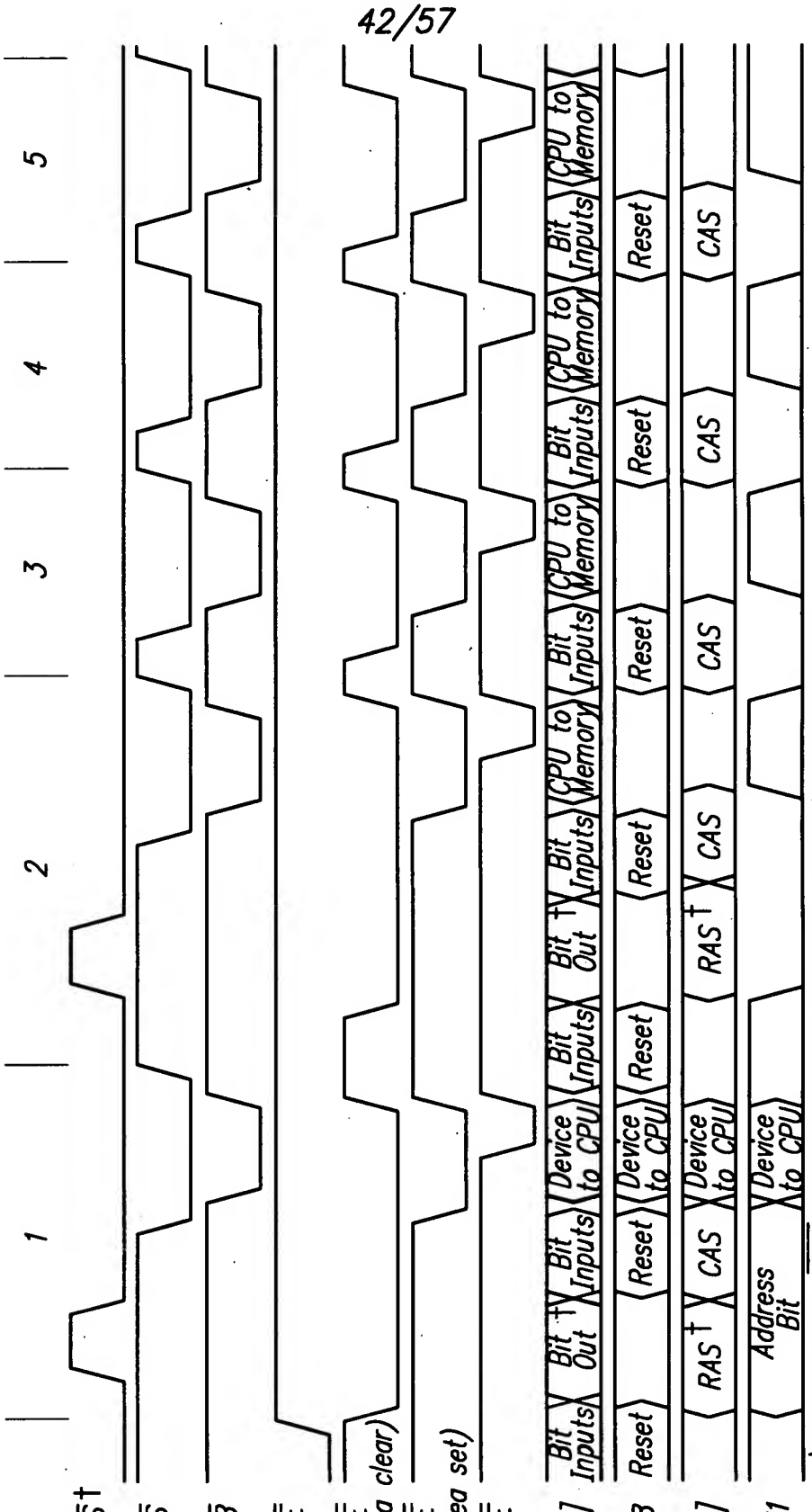

1
2
3
4
5
RAS†
CAS
DOB
OE
EWE (mgbtewea clear)
EWE (mgbtewea set)
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out †
Device to CPU
Reset
RAS †
CAS
Address Bit
CPU to Memory
† Presence of RAS inactive period depends on system conditions.

FIG. 61

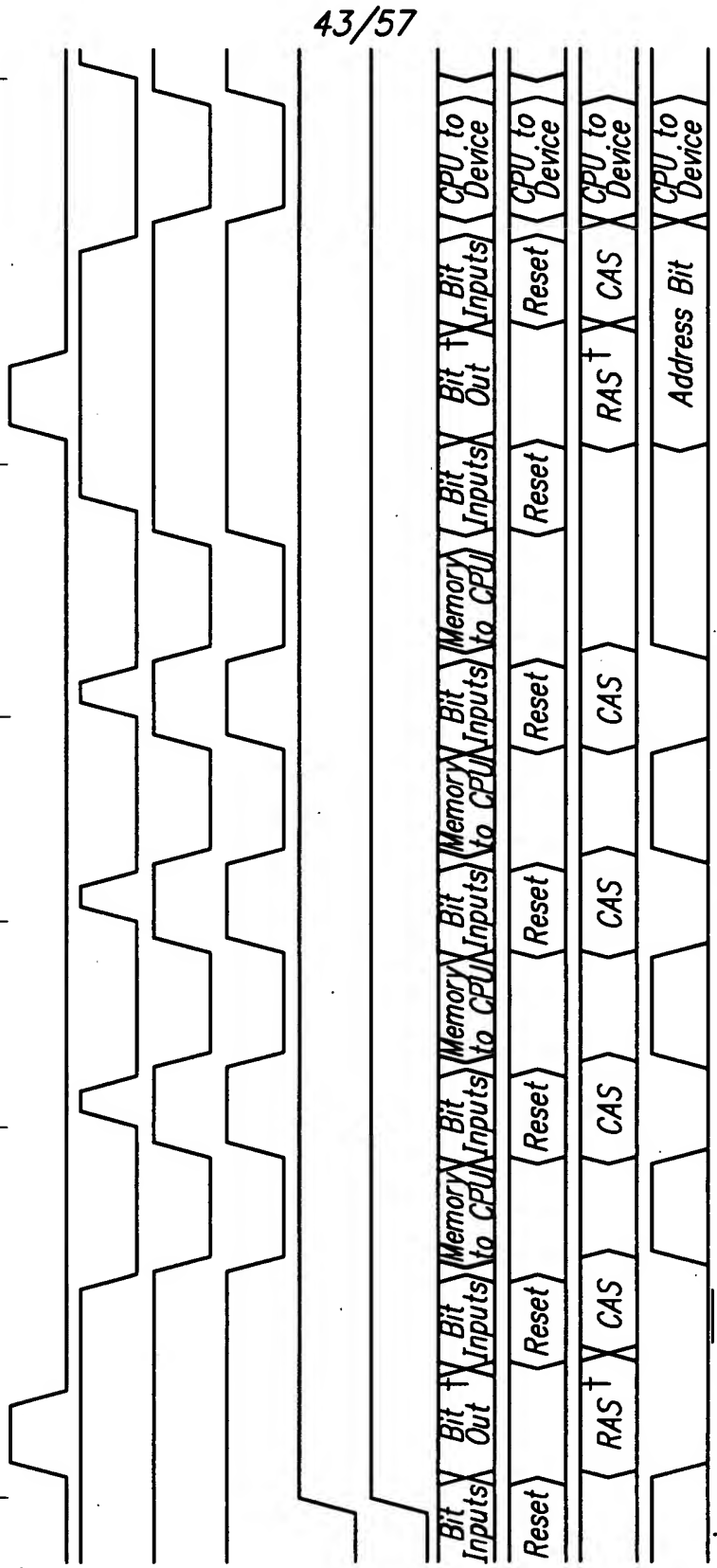

1
2
3
4
5
RAS†
CAS
DOB
OE
EWE
LWE
AD[7:0]
AD8
AD[30:9]
AD31
Bit Inputs
Bit Out †
Memory to CPU
Reset
CAS
RAS †
Address Bit
CPU to Device
† Presence of RAS inactive period depends on system conditions.

FIG. 62

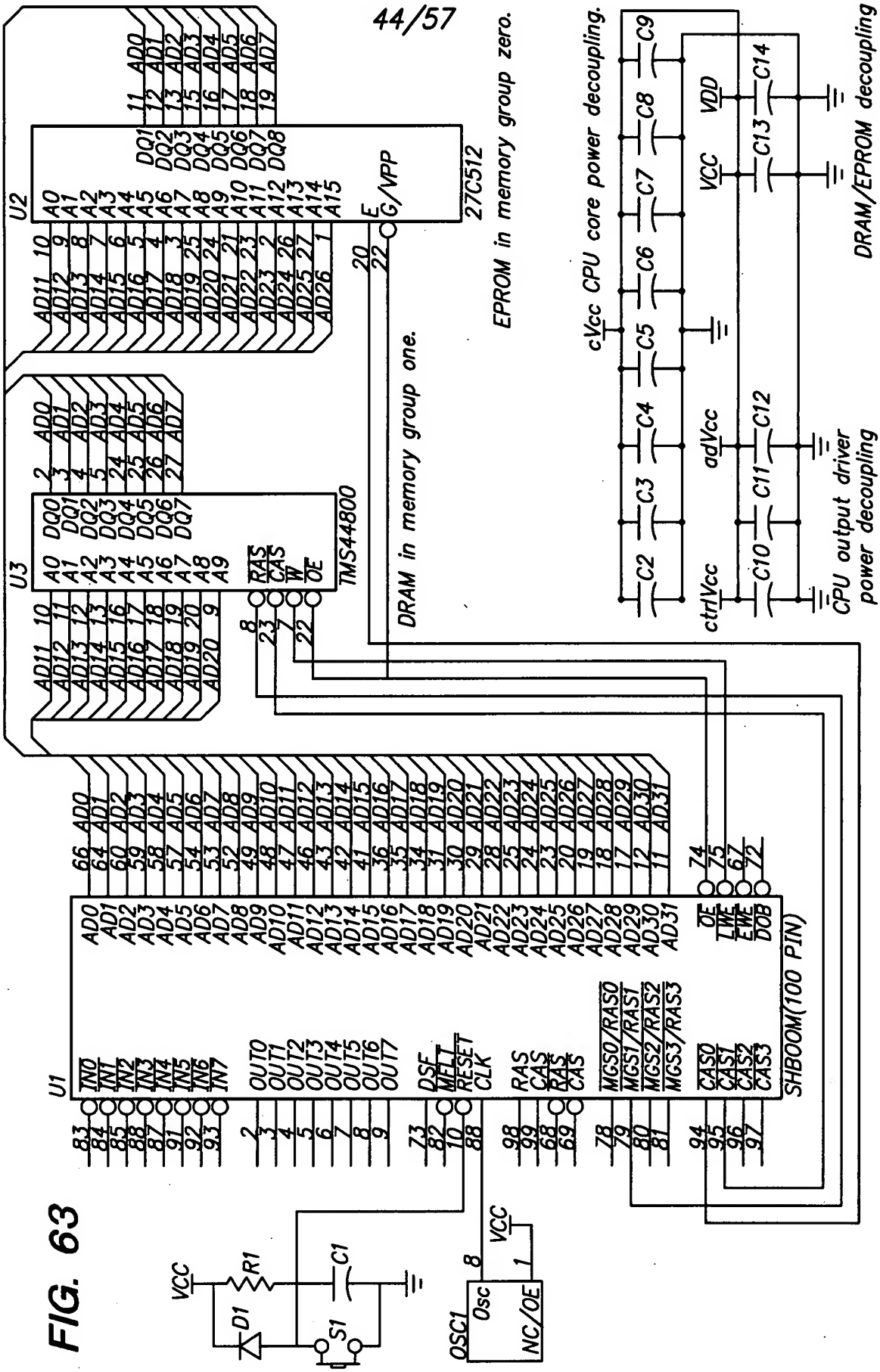

44/57
U1
SHBOOM(100 PIN)
U2
27C512
EPROM in memory group zero.
U3
TMS44800
DRAM in memory group one.
cVcc CPU core power decoupling.
adVcc
ctrlVcc
CPU output driver power decoupling
DRAM/EPROM decoupling
VCC
VDD
R1
C1
D1
S1
OSC1
Osc
NC/OE

FIG. 63

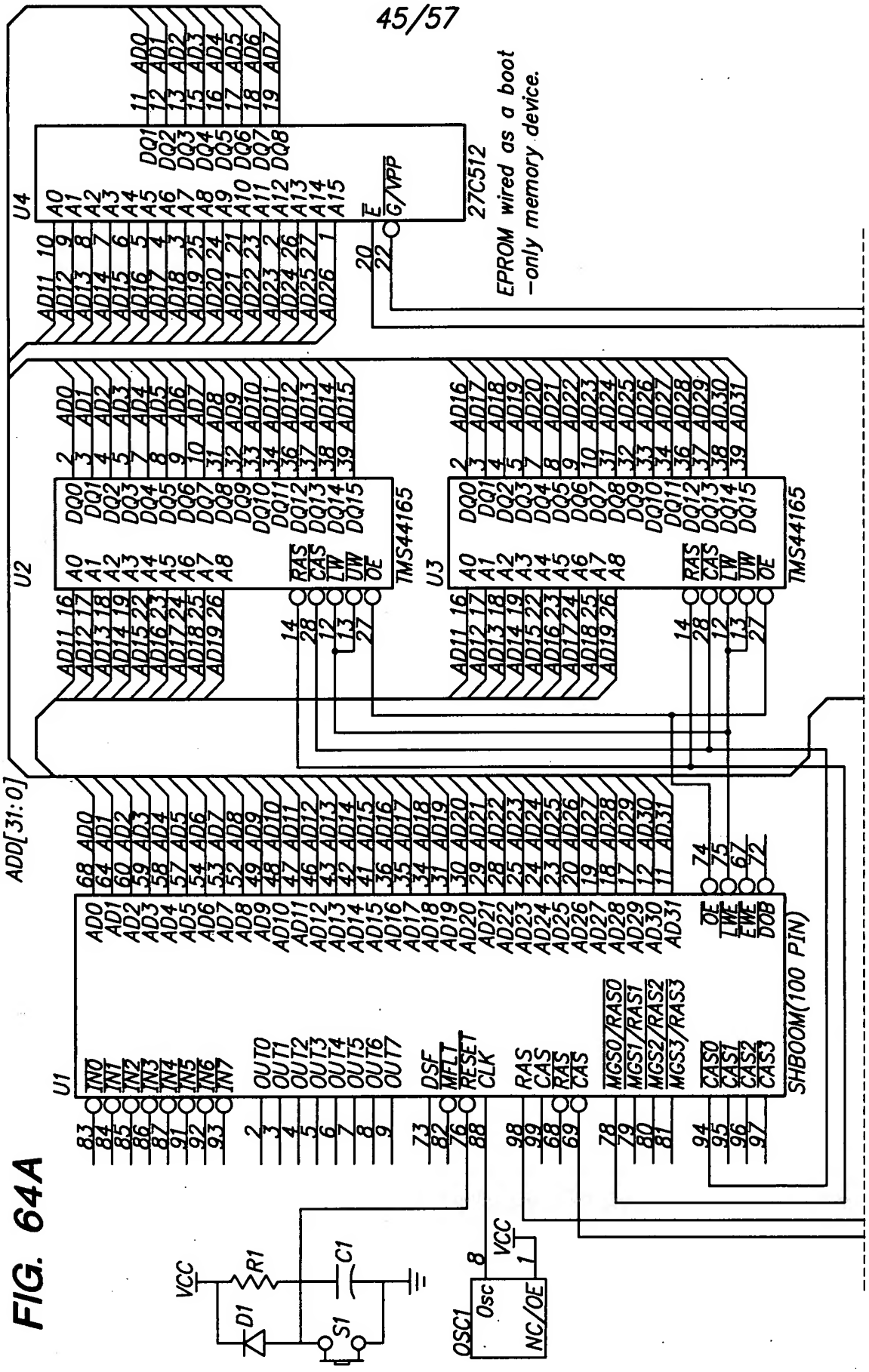

U4
27C512
EPROM wired as a boot
-only memory device.
U2
U3
TMS44165
ADD[31:0]
U1
SHBOOM(100 PIN)
R1
C1
D1
S1
OSC1
Osc
NC/OE
VCC

FIG. 64A

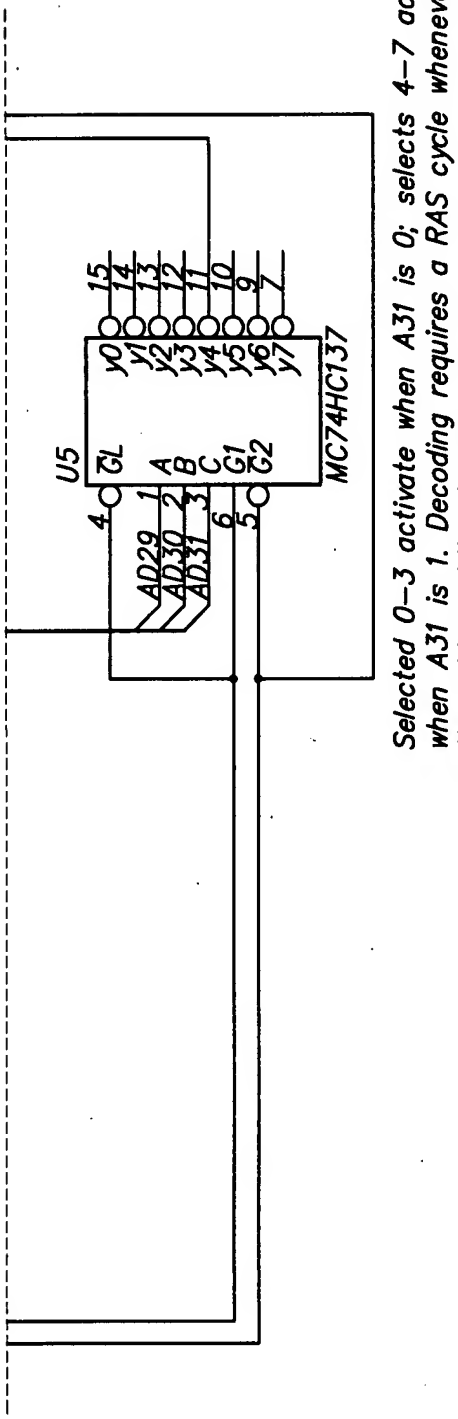


FIG. 64

FIG. 64A	FIG. 64B

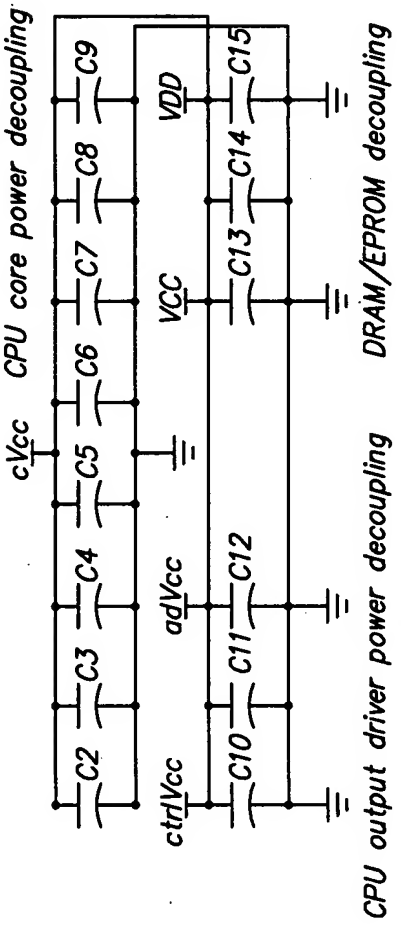


FIG. 64B

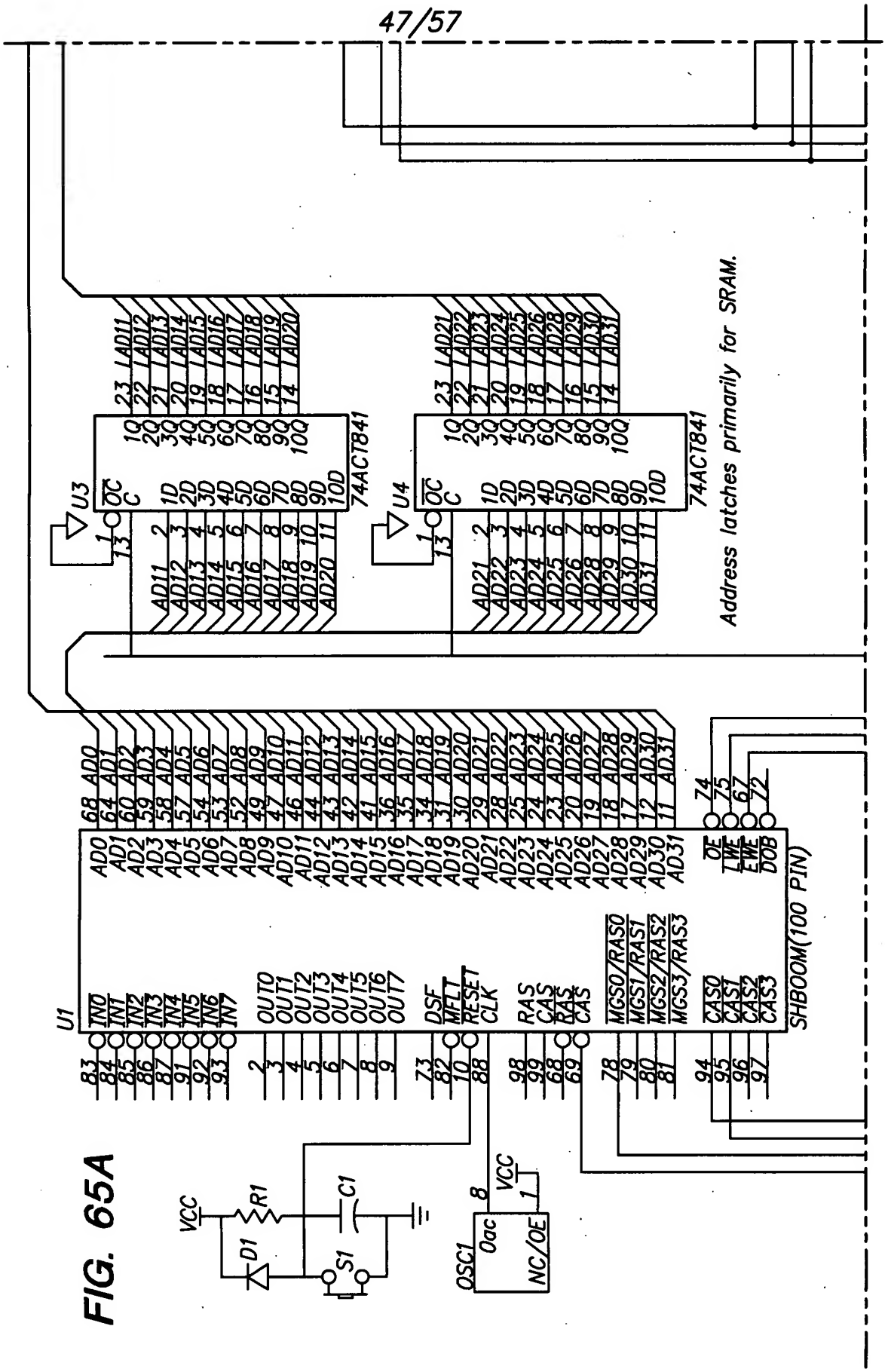

47/57
U3
74ACT841
U4
74ACT841
Address latches primarily for SRAM.
U1
SHBOOM(100 PIN)
VCC
R1
C1
D1
S1
OSC1
Oac
NC/OE

FIG. 65A

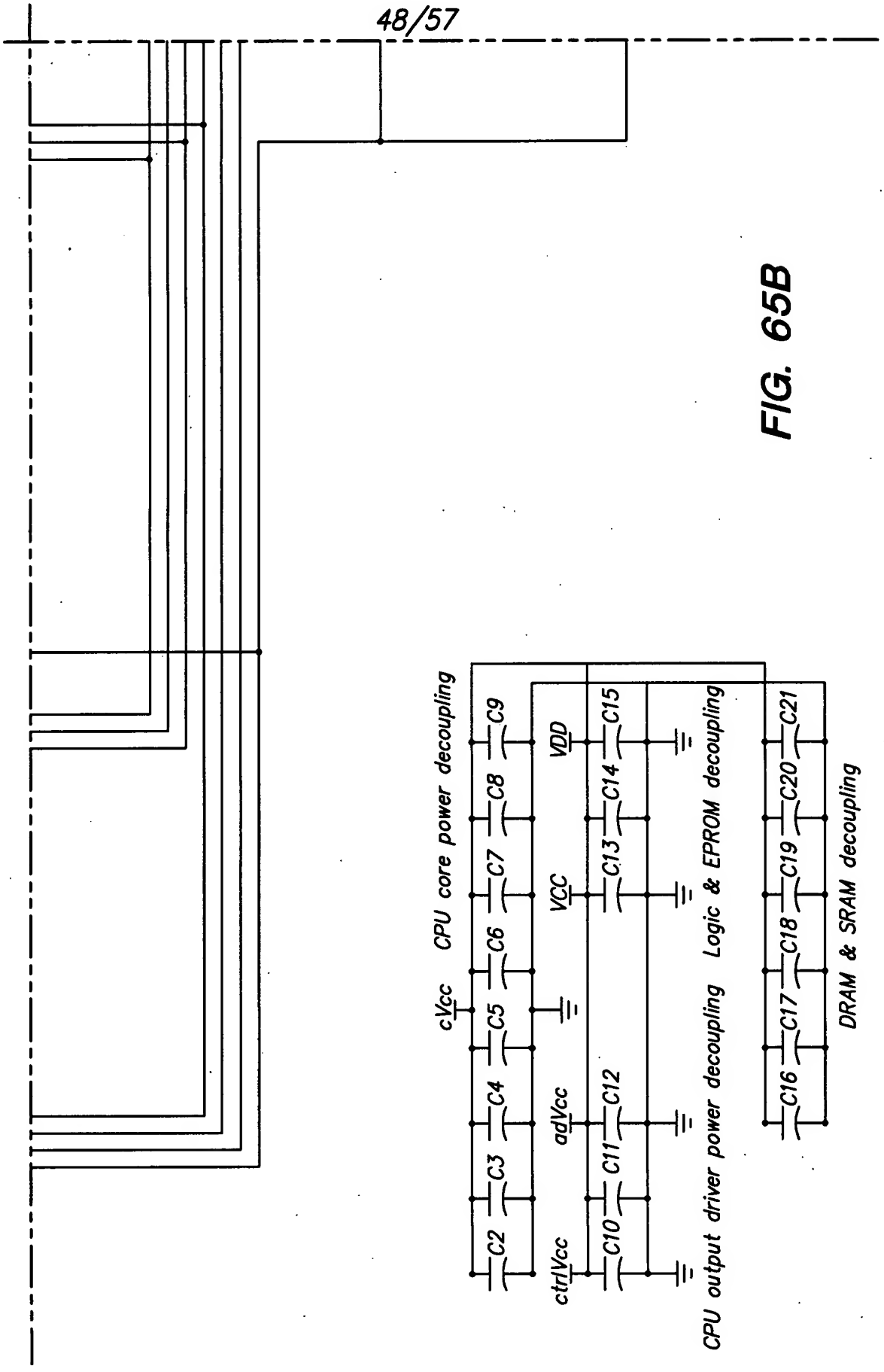

cVcc
CPU core power decoupling
C2
C3
C4
C5
C6
C7
C8
C9
ctrlVcc
adVcc
VCC
VDD
C10
C11
C12
C13
C14
C15
CPU output driver power decoupling
Logic & EPROM decoupling
C16
C17
C18
C19
C20
C21
DRAM & SRAM decoupling

FIG. 65B

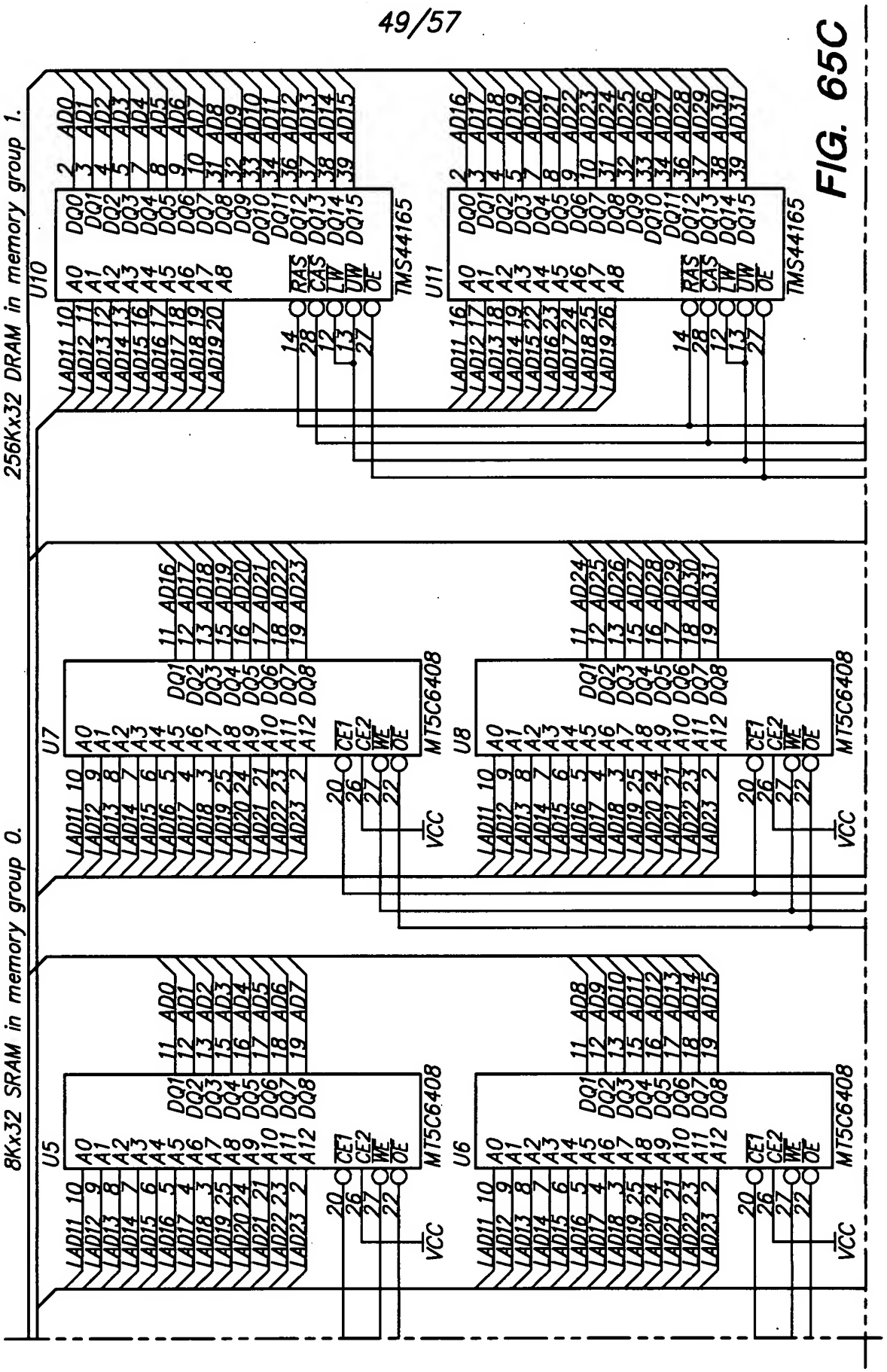

256Kx32 DRAM in memory group 1.
8Kx32 SRAM in memory group 0.
U10
U11
U7
U8
U5
U6
TMS44165
MT5C6408
VCC

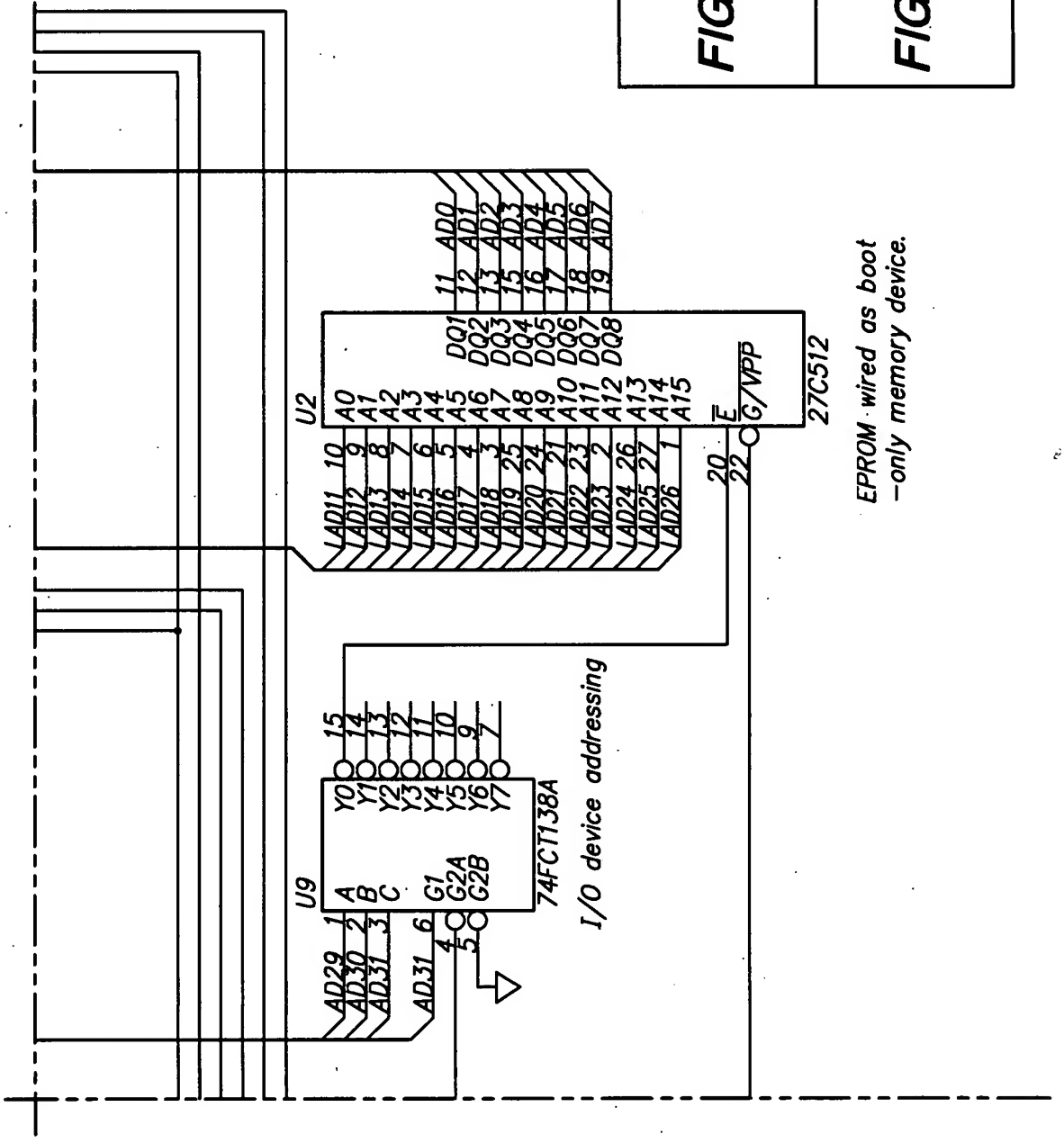
FIG. 65C

50/57

FIG. 65D

FIG. 65

FIG. 65A	FIG. 65C
FIG. 65B	FIG. 65D



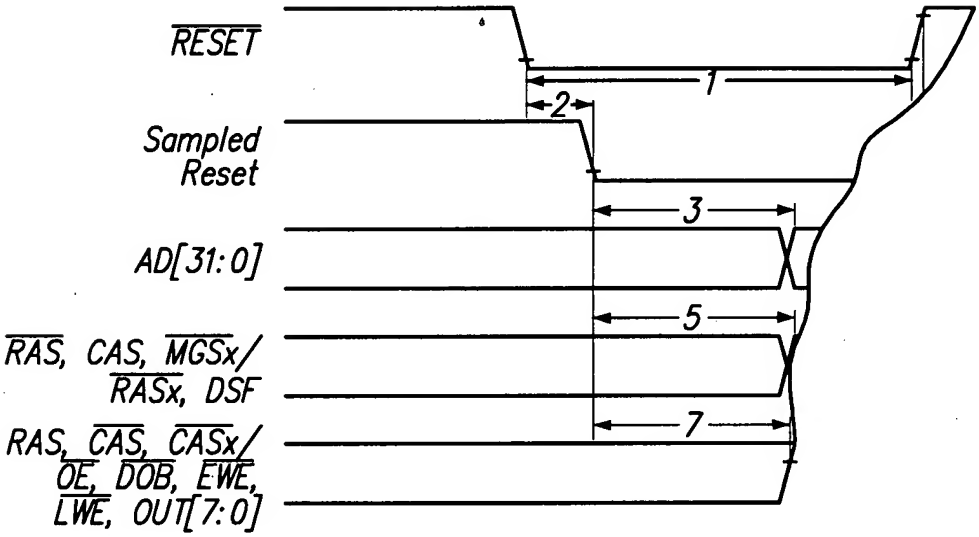

RESET
Sampled Reset
AD[31:0]
RAS, CAS, MGSx/ RASx, DSF
RAS, CAS, CASx/ OE, DOB, EWE, LWE, OUT[7:0]
1
2
3
5
7

FIG. 66

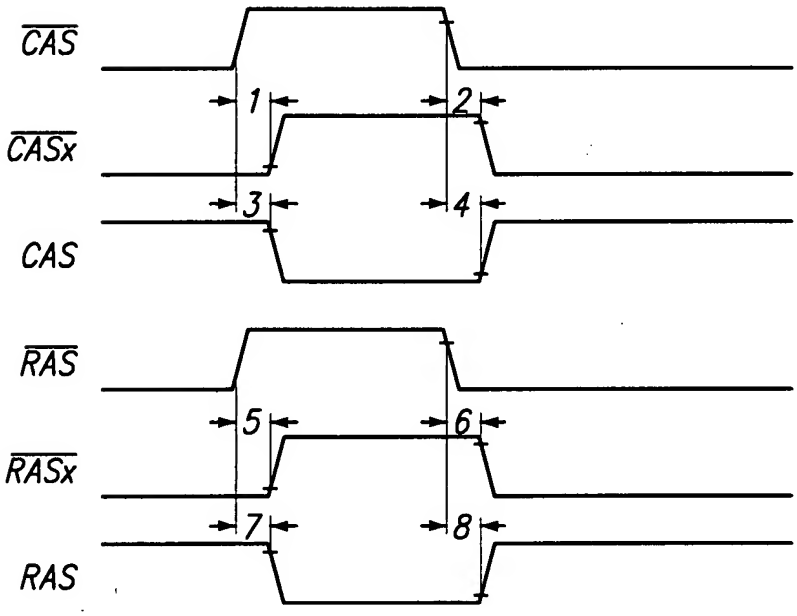

CAS
CASx
CAS
RAS
RASx
RAS
1
2
3
4
5
6
7
8

FIG. 69

52/57

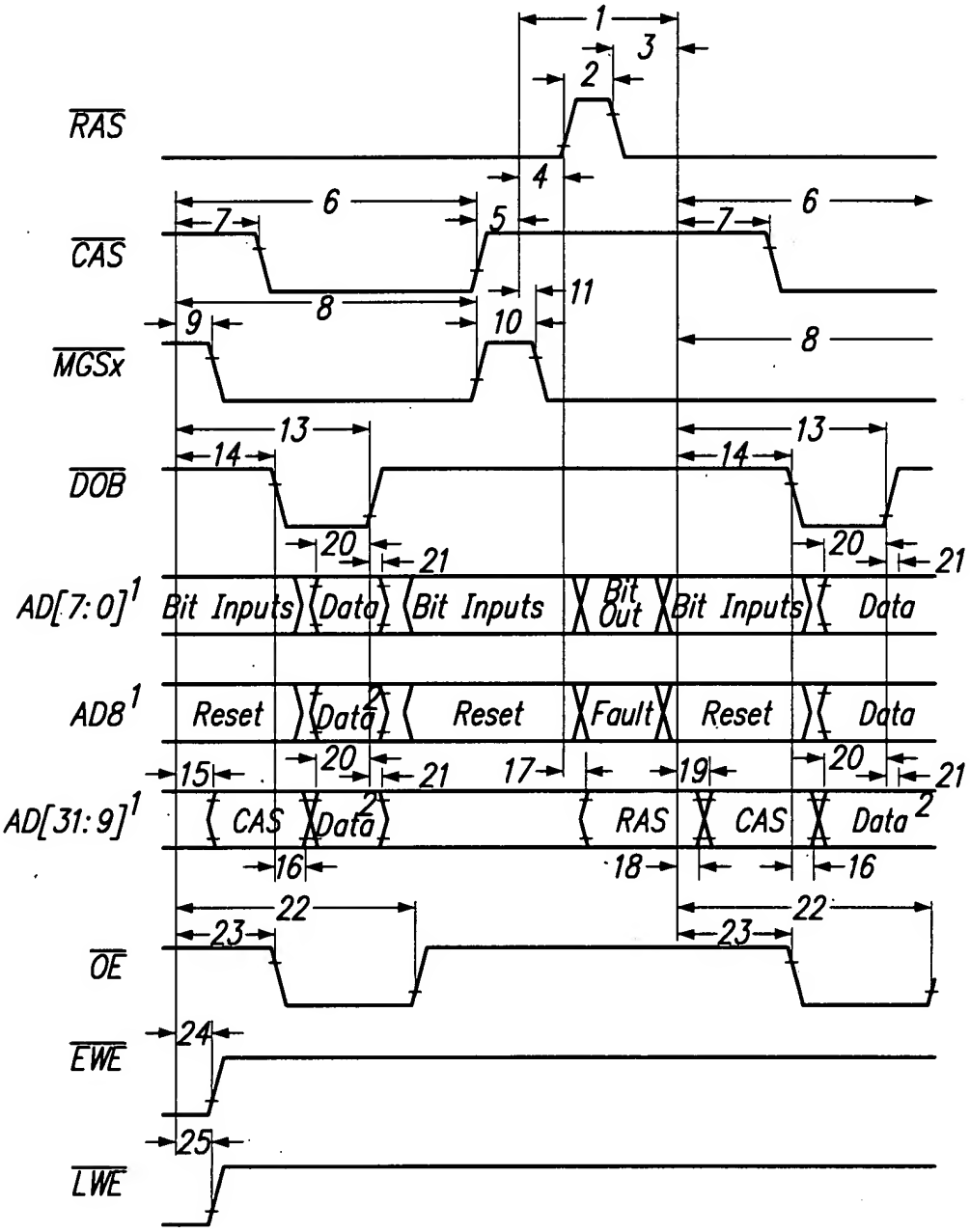

RAS
CAS
MGSx
DOB
AD[7:0]1
AD8 1
AD[31:9]1
OE
EWE
LWE
Bit Inputs
Data
Bit Out
Reset
Fault
CAS
RAS

FIG. 67

53/57

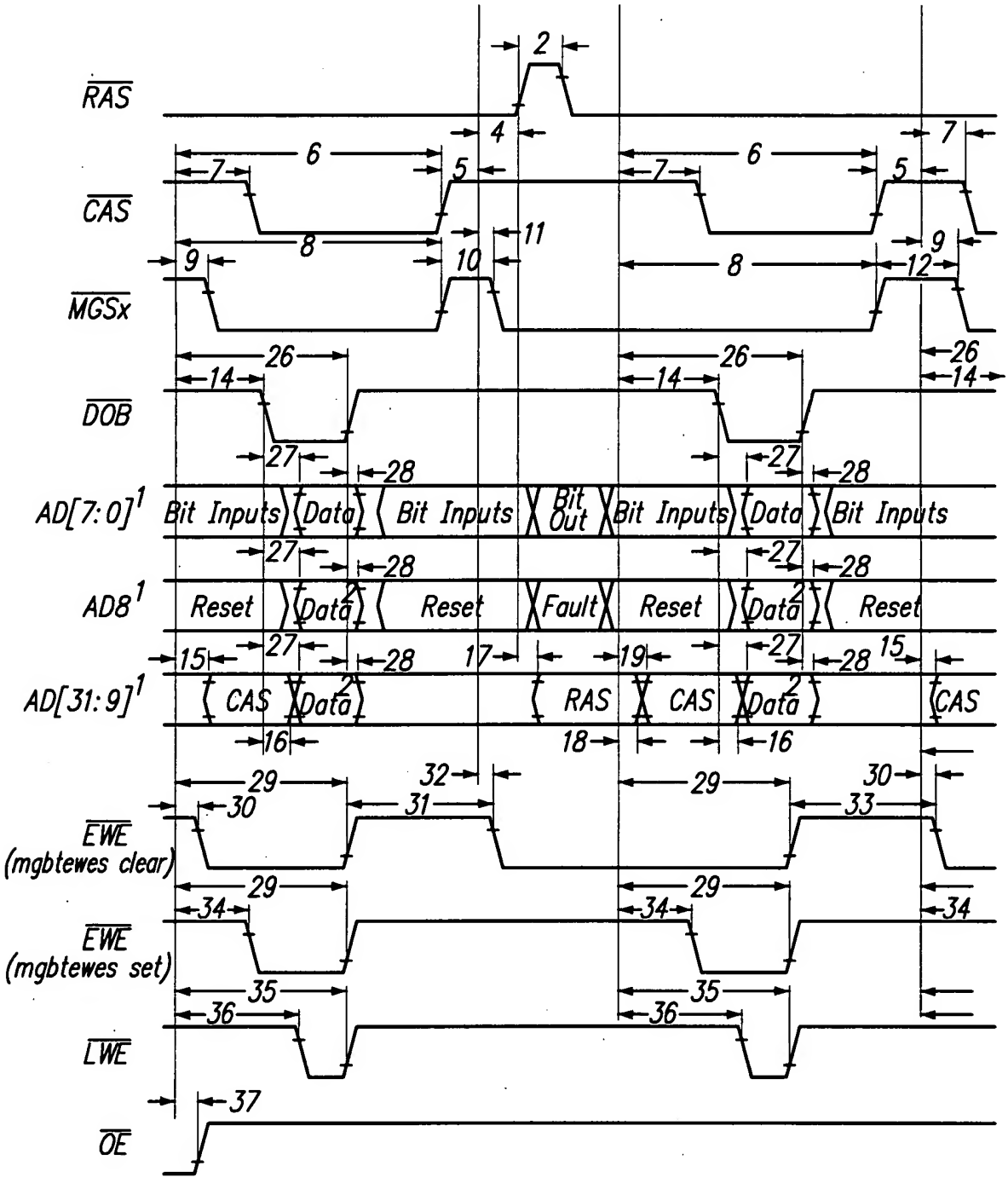

RAS
CAS
MGSx
DOB
AD[7:0]1
AD8 1
AD[31:9]1
EWE (mgbtewes clear)
EWE (mgbtewes set)
LWE
OE
Bit Inputs
Data
Bit Out
Reset
Fault
CAS
RAS

FIG. 68

54/57

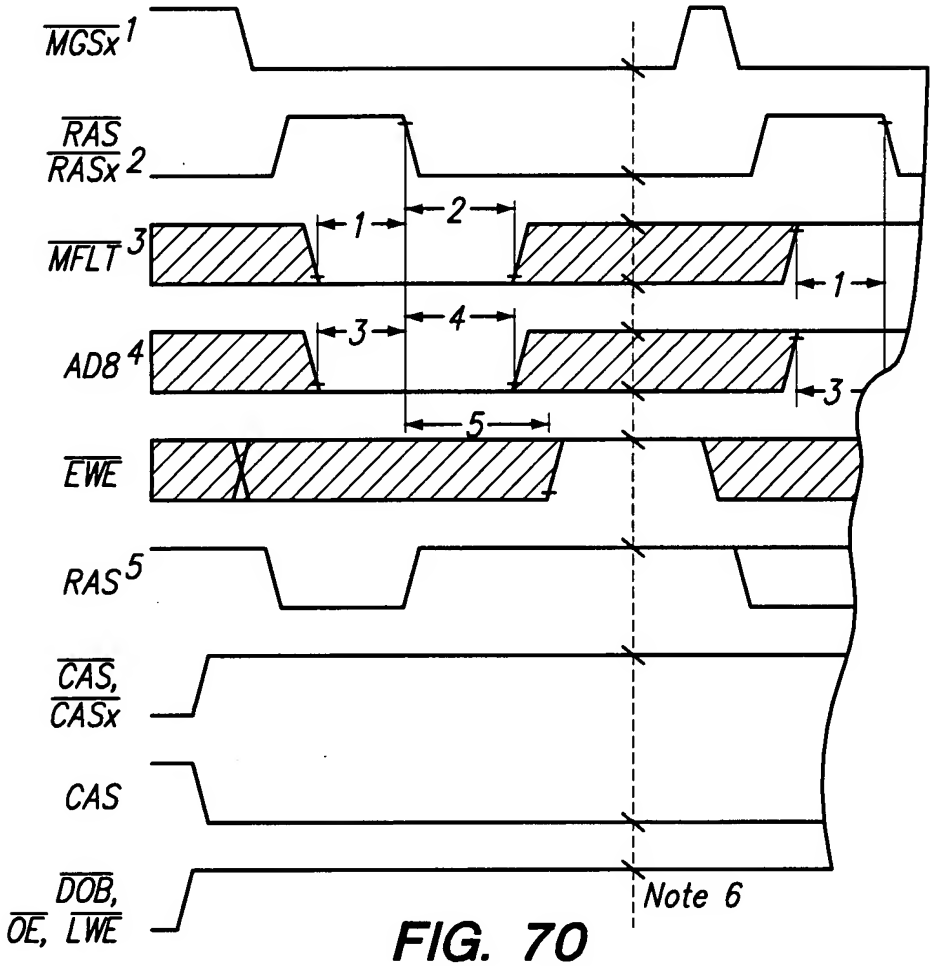


FIG. 70

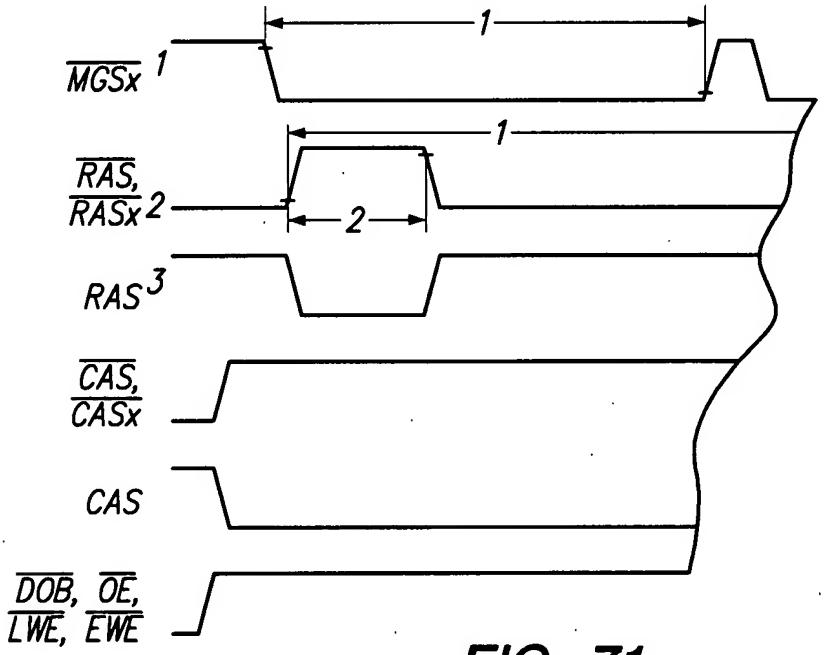


FIG. 71

55/57

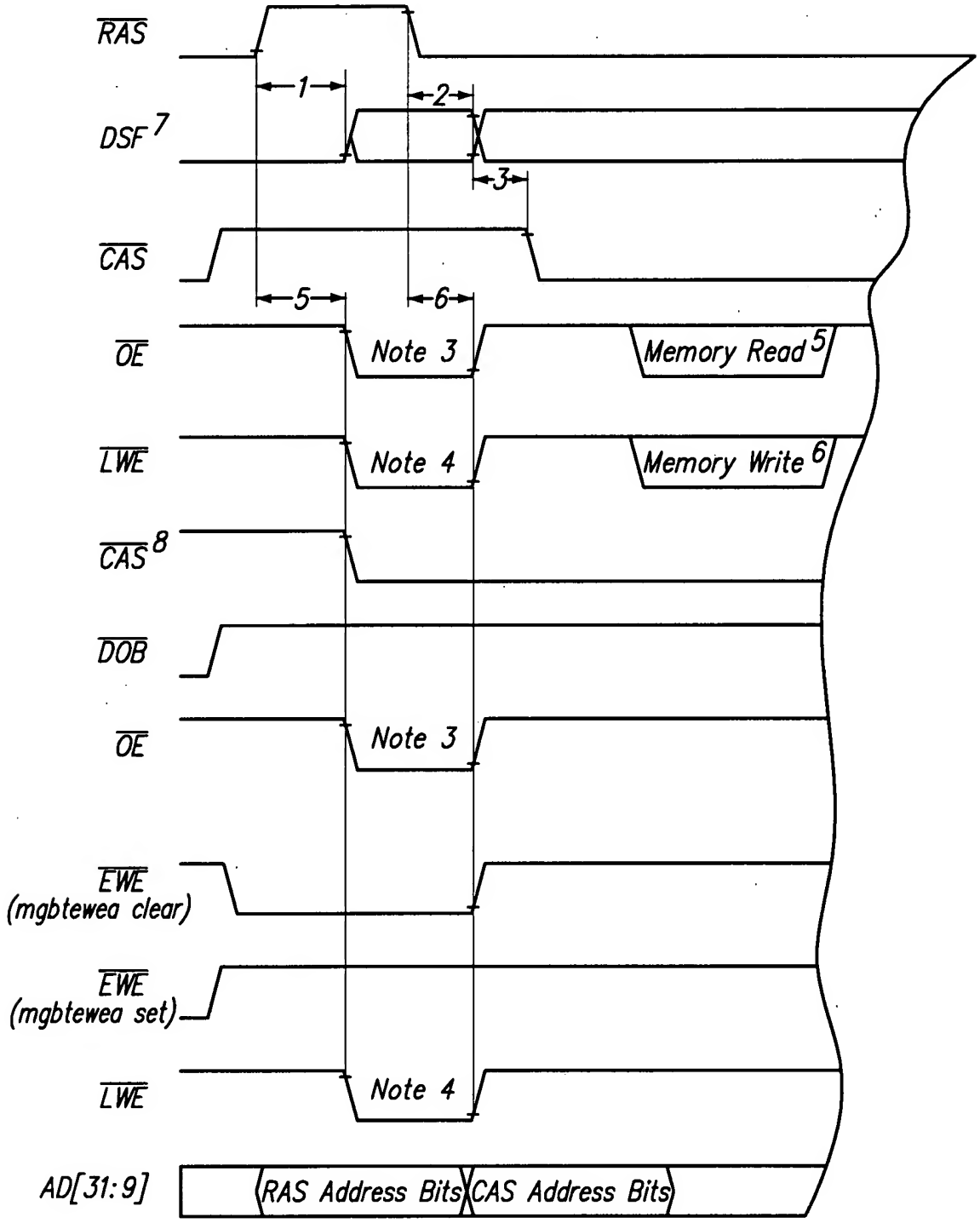

RAS
1
2
DSF 7
3
CAS
5
6
OE
Note 3
Memory Read 5
LWE
Note 4
Memory Write 6
CAS 8
DOB
OE
Note 3
EWE
(mgbtewea clear)
EWE
(mgbtewea set)
LWE
Note 4
AD[31:9]
RAS Address Bits
CAS Address Bits

FIG. 72

56/57

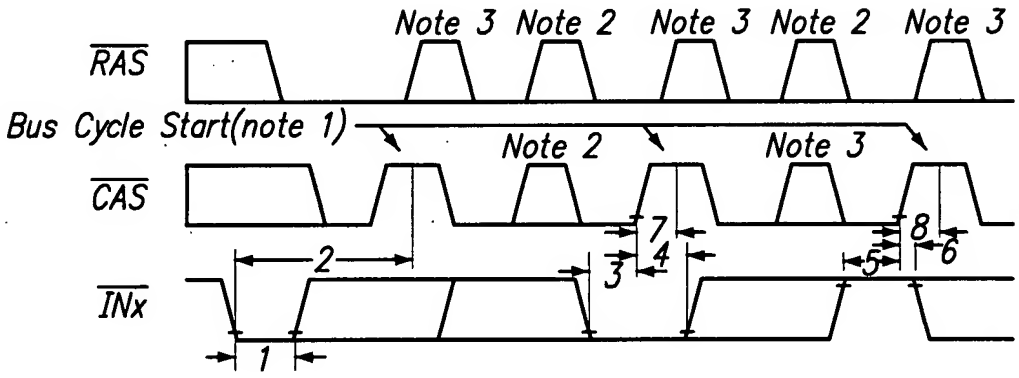


FIG. 73

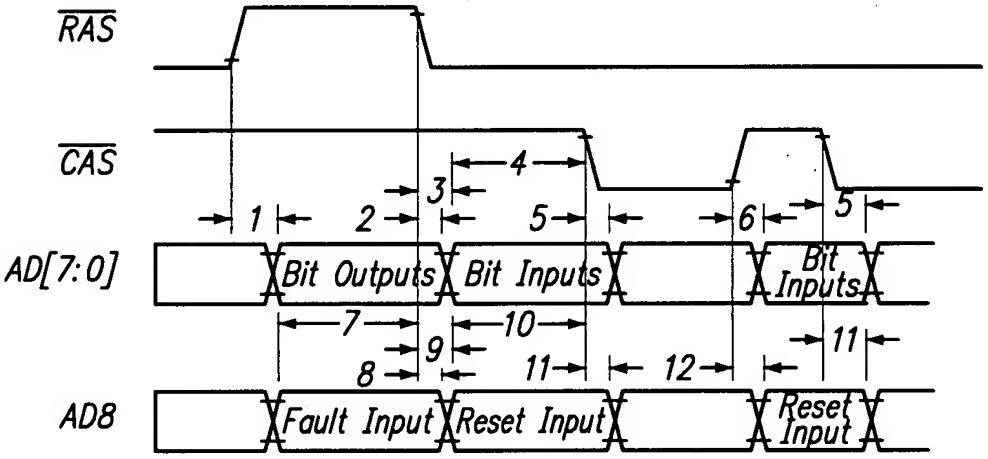


FIG. 74

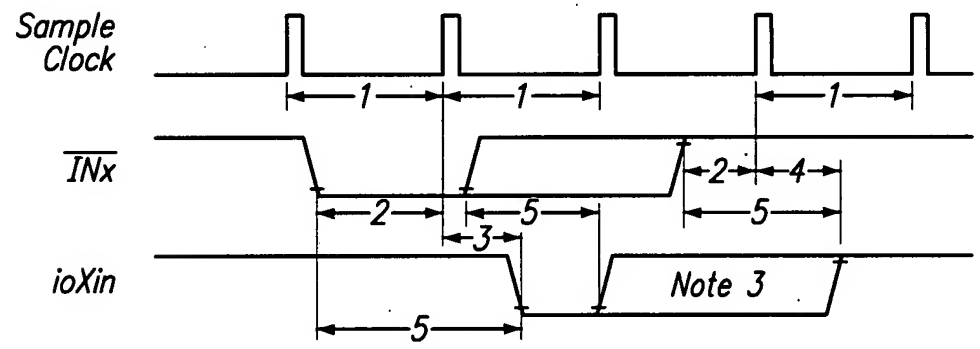


FIG. 75

57/57

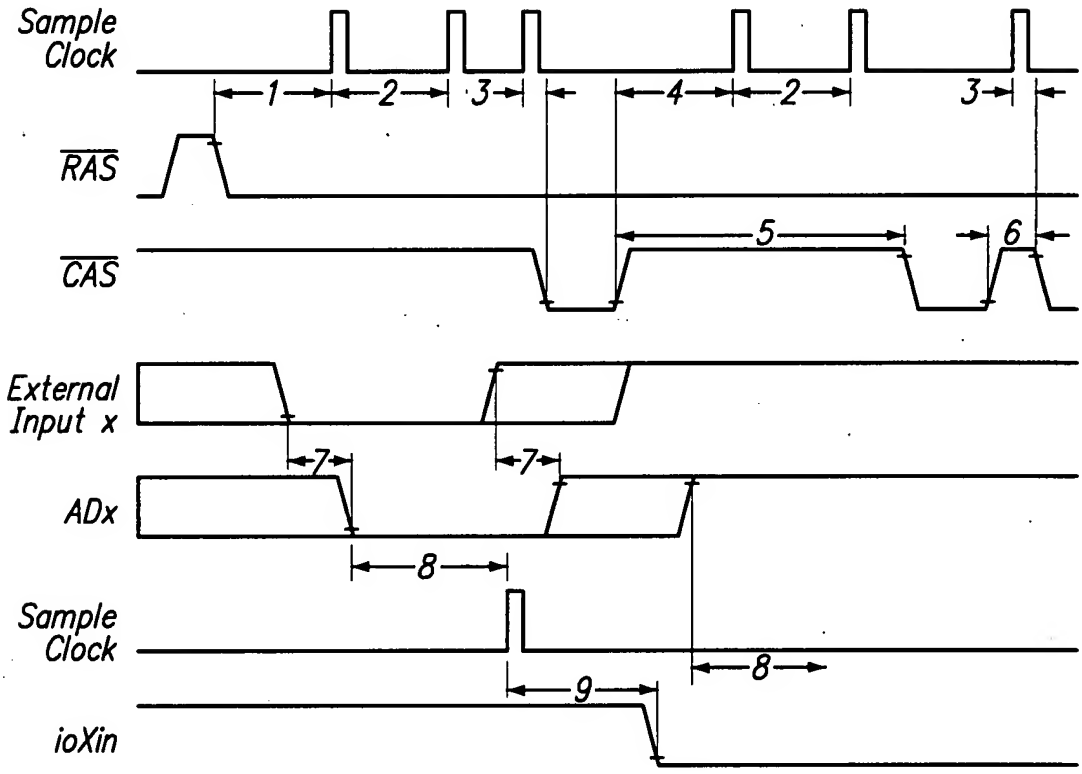

Sample Clock
1
2
3
4
2
3
RAS
5
6
CAS
External Input x
7
7
ADx
8
Sample Clock
8
9
ioXin

FIG. 76